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An Ultra-Low Power SAR-ADC in Ultra-Deep Submicron 32NM CMOS Technology

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Abstract
This paper presents the design and post layout simulation results of SAR based ADC dedicated to ultra-low power, area optimized and high performance applications. In the project experimental work, the CMOS physical SAR based ADC design is designed, simulated and enhanced with the software system tool named Microwind 3.9 EDA tool. We target a 4-bit resolution and a power consumption of few micro Watts. The design has been made through the scaling of device parameters. The design is implemented with operating voltage with core VDD as 1.00 V and IO VDD as 1.80V. The simulations results indicate that the physical design achieves 4-bit conversion and the converter is well suited for operation for 1 V. The proposed SAR ADC draws a small amount of power 1.89 mW and physical area of 809.7µm2.

Keywords: ADC, SAR, CMOS Technology, Low power, comparator, digital-to-analog converter, sample-and-hold, etc.

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I. INTRODUCTION

In the past few years, lot of research activities have been carried out finding innovations and low-cost solutions for the electronics industry [1] [2] [3]. The advancement in the submicron CMOS technology, allow a high level of integration and reduction of cost, many miniaturized devices were developed for multiple applications where power consumption and physical area is very crucial. Among various ADC architectures, the Successive Approximation Register (SAR) ADC exhibits significant advantages compared to other ADC architectures such as pipelining and Delta-Sigma, in terms of power consumption and area. It is the most popular approach for realizing A/D converters, due to its reasonably quick conversion time, moderate circuit complexity, high accuracy, and it's a proper choice for low power applications [2].

ADCs are key components for the design of power limited systems, in order to keep the power consumption as low as possible [1] [5]. The stringent requirements on the energy consumption increase the need for the development of lowvoltage and low power circuit techniques and system building blocks [2]. The scaling down of feature size by the various factors leads to improved performance. Hence, it is important to understand the effects of scaling [1] [2].

In a SAR- ADC, a digital-to-analog converter (internal-DAC) tries to calculate the value of each sample of the input analog signal through successive approximations and comparisons. Based on the ADC resolution, after a specific number of cycles, the digital word being stored in the successive-approximation register (SAR) corresponds to the analog sample with a specific quantization error [5]. It basically generates one bit per clock cycle, the merits are the low area needed for the implementation. ADCs of this type have good resolutions and quite wide ranges.

The up-down counter based SAR architecture allows for high-speed, typically low-power ADCs to be packaged in small form factors for today's high demanding applications. With Microwind EDA Software tool, we have designed 4 bit low power SAR ADC with 45 nm technology.

Along with the same, the trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area. VLSI fabrication technology is leading to smaller line widths and feature size and hence to higher packing density [4] [5]. The scaling down of feature size by the various factors leads to improved performance. Hence, it is important to understand the effects of scaling [2].
Figure 1 and 2 illustrates the block diagram and conversion procedure of converter.

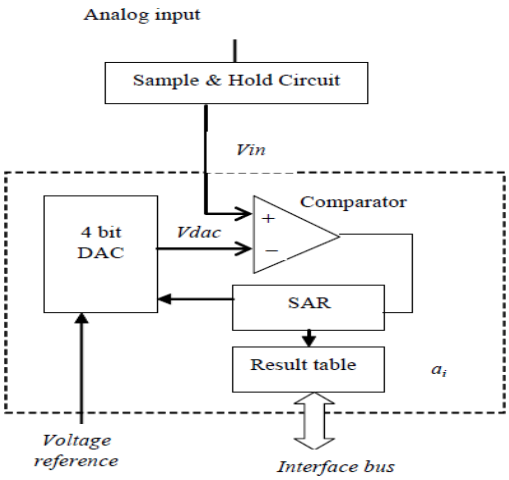

Figure 1: Block diagram of SAR based ADC

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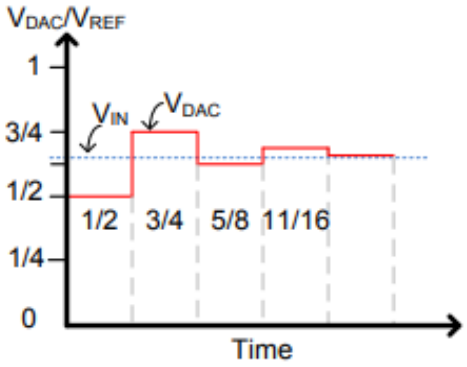

Figure 2: Basic SAR based ADC operation

These values are known as bits with the first voltage that is turned on corresponding to the most significant bit (or MSB) and the last voltage corresponding to the least significant bit (or LSB). When the algorithm finishes the result is a binary code that corresponds to the input voltage. This process is referred to as successive approximation. The ADC resolution is depends on the number of successive approximation cycles. In addition, the resolution is primarily limited by the sensitivity of the comparison block and the accuracy of the D/A converter

1. SAR ADC

The SAR-ADC consists of a sample-and-hold (S/H) circuit, a comparator, a digital-to-analog converter (DAC) and logic control unit. The ADC employs a binary-search algorithm that uses the digital logic circuitry to determine the value of each bit in a successive manner based on the outcome of the comparison between the outputs of the S/H circuit and DAC feedback [1][2][3]. When an input signal is applied to the converter, the comparator simply tells whether the input signal is greater or smaller than the DAC output and gives one digital bit at a time starting from the MSB. The SAR stores the produced digital bit and uses the information to alter the DAC output for the next comparison. This operation is repeated until all the bits in the DAC are decided.

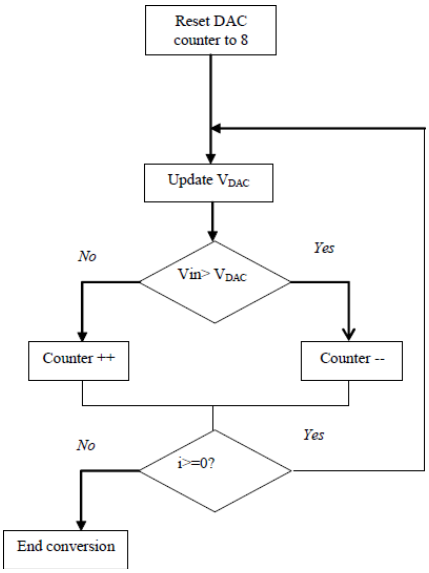

Figure 3: Iterative algorithm for ADC conversion

The SAR algorithm works by switching on a large voltage and comparing that to the input voltage. If the switched voltage proves higher than the input voltage then the algorithm turns off that voltage and turns on a voltage half that size and repeats. If the voltage comes up lower than the input voltage it keeps that voltage on and then adds a voltage that represents half the size of the first voltage and repeats. This then corresponds to a series of 1s and 0s. These values are known as bits with the first voltage that is turned on corresponding to the most significant bit (or MSB) and the last voltage corresponding to the least significant bit (or LSB). When the algorithm finishes the result is a binary code that corresponds to the input voltage. This process is referred to as successive approximation. The code produced results in a readable data form for a computer or micro-controller. Figure 1 below shows the basics of how the algorithm works where VREF represents the max voltage that the SAR ADC can measure.

II. PROPOSED SAR BASED ADC

A. Sample and Hold Circuit

The conversion process of a successive approximation ADC begins at the Sample and Hold circuit. Figure 3 shows the Sample and Hold circuit. Mostly, Sample and hold circuit contains a switch and a capacitor. In the tracking mode, while the sampling signal is high and the switch is connected, it tracks down the analog input signal. In hold mode, it holds the value when the sampling signal changes to low [4]. The value of Cstore is dependent on the number of voltage levels to be observed on the output side.

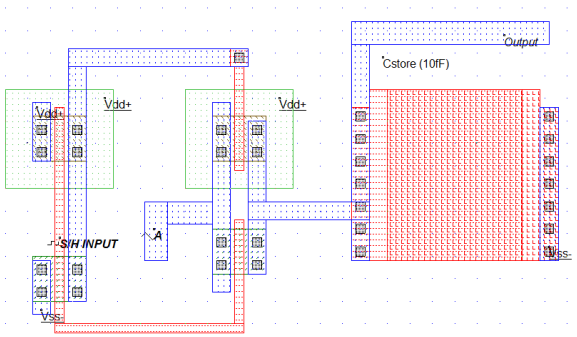

Figure 3: Physical design of Sample and Hold Circuit

B. Comparator

Comparator is the important block of any ADC, It can be said that comparators are fundamental analog to digital converter used to generate one bit of digital data [4] [2]. To optimize the performance of comparator on the basis of high speed, resolution and power dissipation W and L of the used transistors must be taken into consideration.

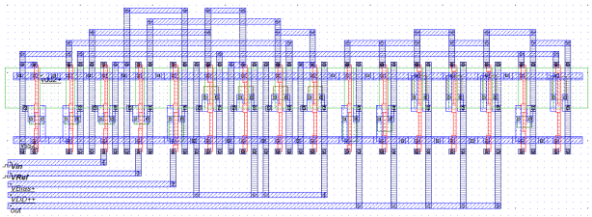

Figure 4: Physical layout High speed comparator

C. Up-Down Counter based SAR Logic Design

The architecture of SAR conversional ADC is shown in Figure.5. A successive approximation register sub block is designed to provide an approximate digital code of Vin to the internal DAC [1] [3]. We proposed a design of SAR counter logic by simplest method, an Up-Down counter to control DAC o/p. It works by starting by binary o/p 8(1000), and then by determining whether Vin is larger or smaller than VDD/2, it decrements or increments. The counter o/p and Vin is compared using comparator which gives the value of that count directly. The comparison is performed for the next count, and so on until all count are checked for below or greater than value 8. The conversion would start with SOC signal and cycle finishes after 8 clock cycles, with active low EOC output.

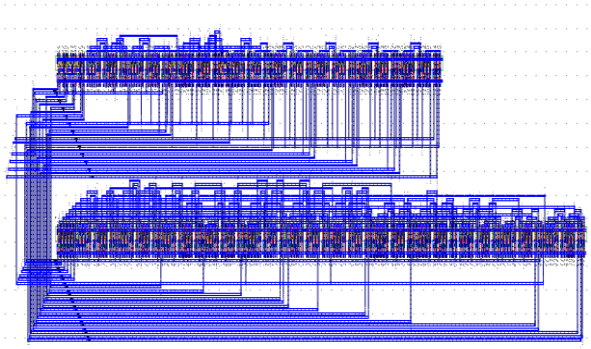

Figure 5: Physical design of SAR Logic

D. Digital to Analog Converter (DAC)

DAC can be implemented using various architectures with varying level of complexity. Each of DAC architecture has its own merits or demerits. Voltage division methods can be used to convert digital code to analog value. R-2R ladder architecture has two operating modes: current mode R-2R ladder and voltage mode R-2R ladder [10]. In this paper, voltage mode R-2R ladder type DAC is used, shown in figure 6.

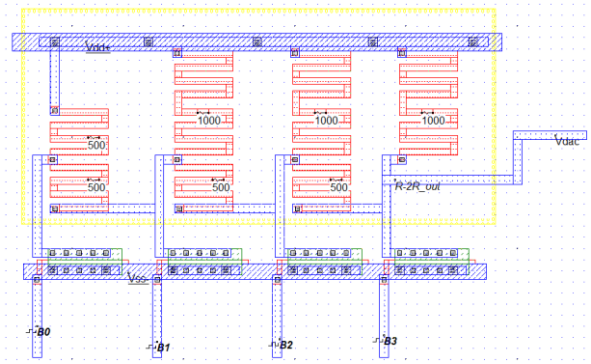

Figure 6: Physical design of R-2R based DAC

III. RESULT AND DISCUSSION

The physical design of all sub-components as Sample and Hold Circuit, Comparator, Up-Down counter based Successive Approximation Register (SAR) and Digital to Analog Converter is implemented and simulated as ADC. The results considering power as a crucial factor shown in table 1 below.

Specification	[1]	[5]	[6]	[9]	**Proposed Work**
Technology Used	45nm	90nm	45nm	90nm	**32 nm**

Architecture	SAR	SAR	SAR	SAR	**SAR**
Resolution (bits)	4 Bits	8 bits	4 bits	4 Bits	**4 Bits**
Supply Voltage (Volts)	1	1.2	1	1.2	**1**
Power Consumption (mW)	4	1.49	2.7	2.59	**1.89**

IV. CONCLUSION

A physical design of 4-bit successive approximation register ADC converter suitable for operation at low supply voltage is designed in a standard 32 nm CMOS technology and compared based on the power dissipation. We implemented Up-Down counter as a SAR logic. The physical design for various internal parts are designed and combined to form a CMOS based ADC. On the input side, we designed Sample and Hold circuit with input as an analog signal. We are trying to design the comparative analysis of the predesigned work with the Up-Down counter based SAR design We have designed a high speed CMOS comparator circuit where the input voltage is swept from 0V to 1 V as Vdd for 45nm technology is 1V. An area efficient DAC architecture based on the R-2R ladder topology is designed. The Results indicate that the physical design achieves 4-bit conversion. Test results indicate that the circuit is well suited for operation for 1 V. The proposed SAR ADC draws a small amount of power 1.89 mW and physical area of 809.7μm2.

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