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Design and Simulation of a Bidirectional Two-Stage DC/DC Converter with Partial Switch Sharing for Vehicle-to-Vehicle Charging Applications

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ABSTRACT: *This study evaluates a 4 kW, 100 kHz isolated bidirectional DC/DC converter for vehicle-to-vehicle (V2V) charging between 1200 V and 400–800 V batteries. Partial switch sharing integrates a four-switch buck–boost stage and a dual active half-bridge converter using six active switches. Duty-cycle and single-phase-shift modulation enable voltage regulation and bidirectional power transfer. Operating modes, steady-state characteristics, component design, and MOSFET zero-voltage-switching current-polarity margins are analyzed. Cascaded PI and PI-assisted 45-rule Mamdani fuzzy controllers are compared in MATLAB/Simulink across four voltage-transfer conditions and 4-to-2 kW power steps. Simulated full-load efficiencies range from 90.55% to 98.06%. Fuzzy control achieves 6–12 ms settling times versus 0.65–0.89 s for cascaded PI. The findings indicate feasible isolated V2V energy transfer and faster simulated transient regulation with fuzzy control.*

NOMENCLATURE

Symbol	Description	Unit
V_{High}, V_{Low}	High- and low-side battery voltages	V
V_2, V_3	Intermediate and secondary voltages	V
i_{L1}, i_{Lr}	Energy-storage and leakage currents	A
L_1, L_r, L_m	Storage, leakage, magnetizing inductance	H
$C_{1–6}$	DC-link and half-bridge capacitance	F
P, P_o	Transferred and rated output power	W
f_{sw}, T_s	Switching frequency and period	Hz, s
D, n	Duty and transformer turns ratios	–
t_d, $t_{0–3}$	Dead time and mode boundaries	s
N_p, N_s	Primary and secondary winding turns	–

Greek letter

φ	Normalized phase-shift ratio	–
θ	Phase-shift angle	rad
Δ	Difference or ripple operator	–
η	Simulated efficiency	%

Subscripts

High, Low	High- and low-voltage sides
p, s	Primary and secondary
dc, sw	DC link and switching
rms, max	Root-mean-square and maximum

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I. INTRODUCTION

Road transportation consumes fossil fuels and contributes to greenhouse gas emissions [1],[2]. Electric vehicles (EVs) offer higher efficiency, lower operating costs, and compatibility with cleaner energy sources [3],[4].

Vehicle-to-Everything (V2X) supports bidirectional EV energy exchange with grids, buildings, loads, vehicles, and ships [5]. Vehicle-to-Vehicle (V2V) charging directly connects EVs without fixed charging infrastructure [6].

Regional development, EV adoption, and investment affect charging accessibility [7],[8]. Rural transportation energy demand is only slightly lower than urban demand [8]. V2V can extend range and provide emergency support where charging infrastructure is unavailable [9].

V2V converter design must combine bidirectionality, high efficiency, compactness, isolation, and wide voltage conversion, which remains challenging [10]. Higher battery voltages require wide-range bidirectional

DC/DC interfaces [11],[12]. High-frequency conversion provides compact high-gain solutions [13], but combining gain, isolation, and low component count is difficult [13],[14]. Semiconductor stress, circulating current, and control complexity also limit conventional isolated converters [15]–[17]. V2V architectures differ in power, interface, isolation, topology, stages, and efficiency. Charging power is commonly classified as Level-1 slow, Level-2 moderate, or Level-3 fast charging [18],[19].

DC-linked V2V solutions are onboard or off-board. Onboard systems reuse vehicle power electronics to reduce conversion stages [20],[21]. Direct DC-link schemes with non-isolated converters have also been studied [22],[23]. These approaches generally offer limited voltage conversion and power transfer; their need for EV DC-link access restricts feasibility in commercial platforms.

Off-board DC V2V uses an external converter between EVs for wider voltage conversion and higher power transfer. Non-isolated multiport bidirectional DC/DC converters connect low-voltage ESSs to 400–800 V EVs for voltage conversion and power sharing [24]. Bridgeless buck–boost and bidirectional DC/DC structures support G2V, V2G, and V2V in SRM-drive EVs [25],[26]. Moderate complexity, high cost under slow charging, or limited soft-switching capability remain limitations [27].

Isolated multi-stage converters offer high gain, galvanic isolation, efficiency, and power density for high-voltage V2V interfaces [28]. The Dual Active Bridge (DAB) is widely used for bidirectional transfer and simple control. Current-fed DAB converters extend gain through an input series inductor [29]. Half-Bridge DAB (HB-DAB), Double Stacked Active Bridge (DSAB), and Partial Parallel DAB (PP-DAB) structures improve efficiency over wide power ranges [30]–[32]. Conventional DAB operation may nevertheless lose ZVS at light load because the current is insufficient to commutate device output capacitances [32].

Partial switch sharing provides a useful basis for integrating voltage regulation with isolated bidirectional conversion. Li et al. [33] demonstrated this approach in an HB^2-DAHB converter for a 400 V onboard bus and 48/24 V auxiliary supplies. Their study established the combined use of duty-cycle and phase-shift modulation in a multiport architecture. The present work develops this architectural basis into a two-port interface for high-voltage battery-to-battery energy transfer and investigates its closed-loop behavior over the 400–1200 V range.

The remainder of this paper is organized as follows. Section II presents the proposed converter topology, operating principle, and ZVS analysis. Section III discusses the steady-state voltage and power-transfer characteristics and component design. Section IV describes the cascaded PI and PI-assisted fuzzy control strategies. Section V reports the MATLAB/Simulink results under full-load bidirectional operation and full-to-half-load transitions. Section VI discusses the comparative results, and Section VII concludes the paper.

II. PROPOSED CONVERTER TOPOLOGY

SYSTEM CONFIGURATION

Fig. 1 shows the 4 kW, 100 kHz interface between 1200 V and 400–800 V batteries. It integrates a four-switch buck–boost (FSBB) and a DAHB stage through a shared leg, providing isolated bidirectional transfer with six active switches. Compared with a full bridge, the DAHB uses fewer devices and SPS control [33],[34].

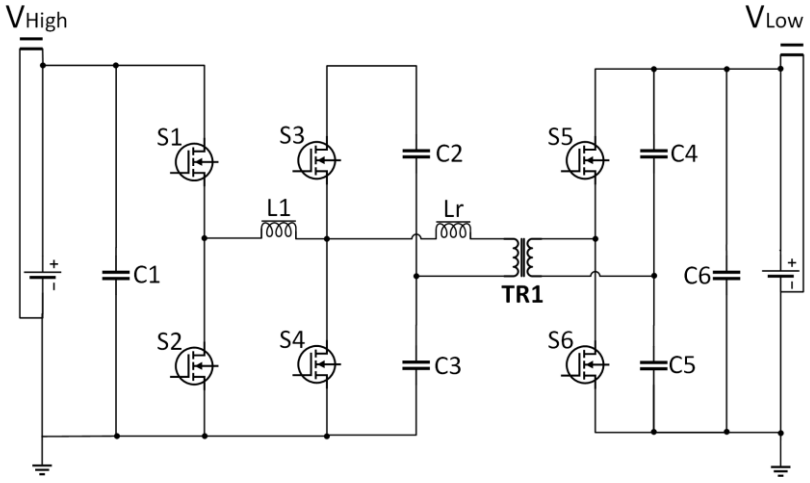


Fig. 1. Bidirectional DC/DC converter topology

OPERATING PRINCIPLE

Fig. 2 illustrates the analytical switching sequence for forward buck operation, with power flowing from the high-voltage to the low-voltage port. Each half-bridge operates complementarily; the auxiliary duty ratio $D <$ 0.5 regulates the DAHB input voltage, while switches S3–S6 retain a 0.5 duty ratio.

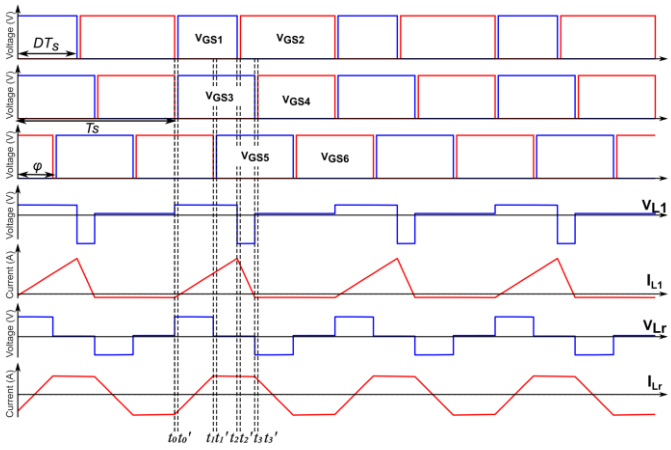


Fig. 2. Key switching waveforms under step-down operation.

Mode 1 (t_0–t_1): Switches S_1, S_3, and S_6 conduct. During the preceding t_0–t_0' deadtime, sufficient reverse L1 current can commutate the S_1–S_2 capacitances for ZVS turn-on of S_1. The negative i_{L_r} current, together with i_{L_1}, supports S3 commutation. At t_0', S_1 and S_3 turn on, and V_{High} supplies the DAHB input V_2 through L_1. The transformer TR_1 primary and reflected secondary voltages are $V_2/2$ and $nV_3/2$, giving $(V_2 + nV_3)/2$ across L_r. The resonant current i_{L_r} follows

$$i_{L_r}(t) = i_{L_r}(t_0) + \frac{V_2 + nV_3}{2L_r}(t - t_0) \tag{1}$$

where $i_{L_r}(t_0)$ is the initial Mode 1 resonant current.

The $(V_{\text{High}} - V_2)$ voltage across L_1 also increases its current while S_1 conducts:

$$i_{L_1}(t) = i_{L_1}(t_0) + \frac{V_{\text{High}} - V_2}{L_1}(t - t_0) \tag{2}$$

Mode 2 (t_1–t_2): S_6 turns off at t_1. Energy in L_r can discharge the S_5 output capacitance, supporting ZVS turn-on of S_5 and continued transfer from V_{High} to V_{Low}.

The approximately balanced primary and reflected secondary voltages produce a quasi-freewheeling interval with nearly constant resonant current:

$$i_{L_r}(t) = i_{L_r}(t_1) + \frac{V_2 - nV_3}{2L_r}(t - t_1) \tag{3}$$

The positive voltage across L_1 throughout Modes 1–2 gives the maximum current at the end of Mode 2:

$$i_{L_1,\max} = i_{L_1}(t_0) + \frac{V_{\text{High}} - V_2}{L_1}(t_2 - t_0) \tag{4}$$

Mode 3 (t_2–t_3): During the t_2–t_2' deadtime of S_1–S_2, positive i_{L_1} can discharge the S_2 capacitance for ZVS. The L_1 voltage reverses to $-V_2$, reducing its current while energy transfer maintains V_2.The voltage polarity across L_r reverses, and i_{L_r} decreases as energy passes through the transformer to the low-voltage side:

$$i_{L_r}(t) = i_{L_r}(t_2) + \frac{V_2 - nV_3}{2L_r}(t - t_2) \tag{5}$$

The condition $V_2 < nV_3$ gives the negative slope in (5). The energy-storage inductor voltage is

$$V_{L_1} = -V_2 \tag{6}$$

The corresponding current decreases as

$$i_{L_1}(t) = i_{L_1}(t_2) - \frac{V_2}{L_1}(t - t_2) \tag{7}$$

In the symmetrical second half-cycle, the L_1 voltage approaches zero and its current remains near the minimum. The remaining intervals repeat Modes 1–3 with complementary switch states.

ZVS ANALYSIS

Fig. 3 presents the turn-on current-polarity margins of the six MOSFETs over 400–800 V and 2–4 kW. The duty ratio D is obtained from (14), and a positive margin denotes the current polarity required for ZVS turn-on, following Li et al. [33].The energy-storage-inductor extrema and resonant-current terms used in the voltage-power sweep are

$$i_{L_1,v} = \frac{P}{2DV_{\text{High}}} - \frac{\Delta i_{L_1}}{2}, \quad i_{L_1,p} = \frac{P}{2DV_{\text{High}}} + \frac{\Delta i_{L_1}}{2}$$
$$I_{r,\text{sh}} = \frac{V_{\text{Low}}\phi}{4L_r f_{\text{sw}}}, \quad I_{r,\text{sec}} = \frac{V_{\text{Low}}\phi}{2L_r f_{\text{sw}}} \tag{8}$$

The corresponding ZVS-polarity margins are

$$M_{S_1} = -i_{L_1,v}, \quad M_{S_2} = i_{L_1,p}$$
$$M_{S_3} = I_{r,\mathrm{sh}} - i_{L_1,p}, \quad M_{S_4} = I_{r,\mathrm{sh}} + i_{L_1,p}$$
$$M_{S_5} = I_{r,\mathrm{sec}}, \quad M_{S_6} = I_{r,\mathrm{sec}} \tag{9}$$

Fig. 3(a) shows the auxiliary leg. S2 retains a positive margin over the full range, whereas S1 loses the required polarity toward the high-voltage/light-load region. This is consistent with the optimal 100 µH L1 selected to reduce current ripple: the larger inductance reduces the reverse-current excursion available for S1 commutation and narrows its ZVS-polarity region.

Fig. 3(b) shows the partial switch-sharing leg. Although S3–S4 are shared between the regulation and isolated stages, S4 remains in the positive-margin region throughout the investigated range and S3 retains the required polarity over most operating points, with only a limited high-voltage/light-load boundary. Thus, partial switch sharing reduces the active-switch count while largely preserving shared-leg ZVS capability.

Fig. 3(c) shows full-range positive margins for both S5 and S6 over 400–800 V and 2–4 kW. Their equal margin magnitudes follow from the complementary half-cycle symmetry of the secondary half bridge.

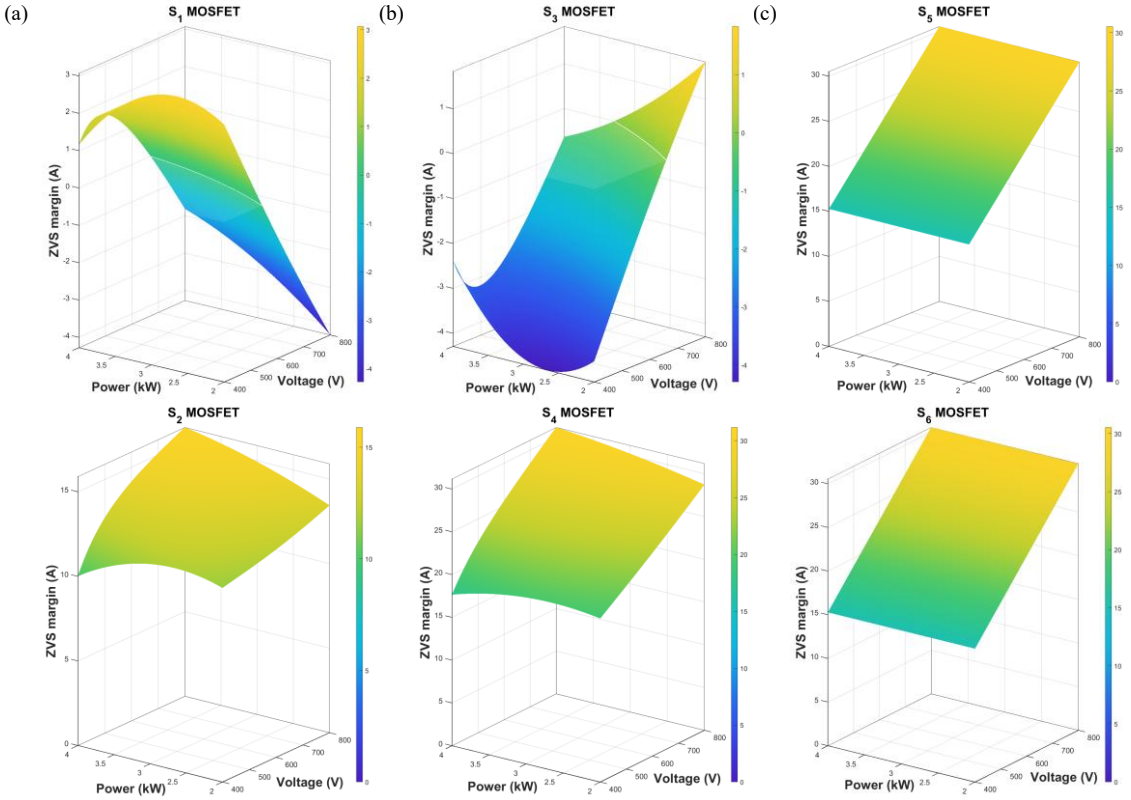


Fig. 3. Analytical ZVS current-polarity margins: (a) auxiliary leg, S1–S2; (b) partial switch-sharing leg, S3–S4; and (c) secondary leg, S5–S6. In each panel, the first switch is shown above the second.

III. STEADY-STATE ANALYSIS

Symmetry permits half-cycle steady-state analysis. The periodic L_1 current satisfies

$$i_{L1}(t_0) = i_{L1}(t_3) \tag{10}$$

Volt-second balance across L_1 over the analyzed half-cycle gives

$$(V_{High} - V_2)DT_s - V_2\left(\frac{T_s}{2} - DT_s\right) = 0 \tag{11}$$

where DT_s and $\left(\frac{T_s}{2} - DT_s\right)$ are the durations of Modes 1–2 and Mode 3. The intermediate voltage is therefore

$$V_2 = 2DV_{High} \tag{12}$$

POWER-TRANSFER ANALYSIS

Power transfer through the leakage inductance L_r is obtained from

$$P = \frac{2}{T_s}\int_0^{t_3} v_{ab}\,(t) i_{L_r}(t)\,dt \tag{13}$$

Substituting the Mode 1–3 currents and imposing steady state yields

$$P = \frac{nV_{High}V_{Low}D}{4L_r f_{sw}}\phi(1-\phi) \tag{14}$$

where V_{High} and V_{Low} are the port voltages, n the turns ratio, L_r the leakage inductance, f_{sw} the switching frequency, D the auxiliary duty cycle, and ϕ the normalized phase shift.

COMPONENT DESIGN

Table 1 lists the specifications and component values selected from the steady-state relationships.

Table 1. Design Parameters of the Proposed Converter

Parameter	Value	Unit
V_{High}	1200	V
V_{Low}	400–800	V
P	4000	W
f_{sw}	100	kHz
t_d	200	ns
C_1, C_6	47	μF
L_1	100	μH
L_r	55	μH
L_m	3.34	mH
n	2:1	-
$C_2 - C_5$	100	μF

DC-Link Capacitor. Capacitors C_1 and C_6 limit bus-voltage ripple to 5% of nominal voltage. The required capacitance is estimated as [35]

$$C_{dc} = \frac{P_o}{2f_{sw}V_{dc}\Delta V_{dc}} \tag{15}$$

A 47 μF value is selected. In (15), P_o is rated power, V_{dc} bus voltage, and ΔV_{dc} allowable ripple.

HF Transformer Design. The high-voltage bus and nominal low-voltage battery determine the turns ratio:

$$n = \frac{N_p}{N_s} = \frac{V_2}{V_{\mathrm{LV}}} = \frac{2D\,V_{\mathrm{High}}}{V_{\mathrm{LV}}}\Big|_{D=0.5} = \frac{1200}{600} = 2 \tag{16}$$

A preliminary analytical design uses an EE8020 ferrite core with $A_e = 404\ \mathrm{mm}^2$, $A_w = 2372\ \mathrm{mm}^2$, and $V_e = 77298\ \mathrm{mm}^3$. For the half-bridge winding voltage $V_2/2$, the minimum primary turn number is

$$N_{p,\min} = \frac{V_p}{4f_{sw}B_{\max}A_e}. \tag{17}$$

With a worst-case winding voltage of 600 V, $f_{sw} = 100$ kHz, and $B_{\max} = 0.15$ T, (17) gives $N_{p,\min} \approx 24.8$. The selected 28:14 winding limits peak flux density to approximately 0.133 T. The modeled $L_m = 3.34$ mH requires $A_{L,\mathrm{target}} = L_m/N_p^2 = 4.26\ \mu\mathrm{H/turn}^2$, close to the nominal core value.

The permissible current density determines the copper cross section:

$$A_{\mathrm{Cu}} \geq \frac{I_{\mathrm{rms}}}{J}. \tag{18}$$

Using $J = 3\ \mathrm{A/mm}^2$ gives primary and secondary copper areas of $6.67\ \mathrm{mm}^2$ and $13.33\ \mathrm{mm}^2$. At 100 kHz, the skin depth is approximately 0.21 mm; the selected Litz-strand diameters, 0.15 mm and 0.12 mm, are below this value. Estimated window utilization is 13.8%, leaving margin for insulation and inter-winding clearance. First-order winding and core losses are estimated from

$$P_{\mathrm{Cu}} = I_{p,\mathrm{rms}}^2 R_{\mathrm{ac},p} + I_{s,\mathrm{rms}}^2 R_{\mathrm{ac},s}, \qquad P_{\mathrm{core}} = p_v(f_{sw}, B_{\max})V_e, \tag{19}$$

where R_{ac} is high-frequency winding resistance and p_v is core-loss density from the material data. Under the EE8020 worksheet assumptions, the winding and core losses are 4.08 W and 7.73 W, totaling approximately 11.81 W.

Leakage Inductor Design. The DAHB energy-transfer inductance L_r follows by rearranging (14) for L_r:

$$L_r = \frac{nV_{High}V_{Low}D}{4f_{sw}P}\phi(1-\phi) \tag{20}$$

For rated transferred power P and the design operating conditions, 55μH is selected.

Energy Storage Inductor Design. Inductor L_1 supports continuous current and the intended soft-switching operation. Its ripple during Modes 1–2 is

$$\Delta i_{L_1} = \frac{1}{L_1}\int_0^{DT_s} \left(V_{\text{High}} - V_2\right) dt \tag{21}$$

For constant applied voltage during this interval, (21) becomes

$$\Delta i_{L_1} = \frac{\left(V_{\text{High}} - V_2\right)D}{L_1 f_{sw}} \tag{22}$$

Substituting (12) and solving for L_1 gives

$$L_1 = \frac{V_{\text{High}} D(1-2D)}{\Delta i_{L_1} f_{sw}} \tag{23}$$

where Δi_{L_1} is the peak-to-peak energy-storage-inductor current ripple.

IV. CONTROL STRATEGY

CLOSED-LOOP CONTROL IMPLEMENTATION

The hybrid controller uses auxiliary duty cycle D to regulate the intermediate bus and DAHB phase shift ϕ to select power-flow direction. The outer voltage PI loop processes the low-voltage bus error to obtain a normalized power demand, which is multiplied by rated power. A step-up compensation term maintains the desired high-voltage-side power. Dividing the power reference by measured low-voltage bus voltage gives the current reference. The inner loop compares this reference with absolute battery current, enabling regulation in either direction.

CASCADED PI CURRENT-MAGNITUDE CONTROL

The cascaded implementation in Fig. 4 uses a PI controller for the inner current-magnitude loop.

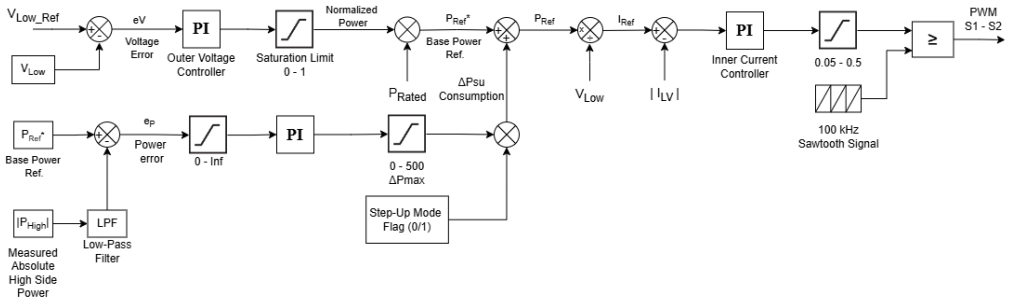


Figure 4. Cascaded PI control structure.

FUZZY LOGIC CONTROLLER

The PI-assisted fuzzy controller retains the outer voltage PI loop and replaces the inner PI with Mamdani inference. Five current-error sets, three voltage-gain sets, and three normalized-power sets give 45 rules. Table 2 specifies the membership functions, input ranges, and four duty-cycle regions. Voltage gain and power select the admissible duty region in Table 2(b); current error adjusts the command within that interval. This confines transient duty variation to the selected operating region. Fig. 5 shows the resulting control structure.

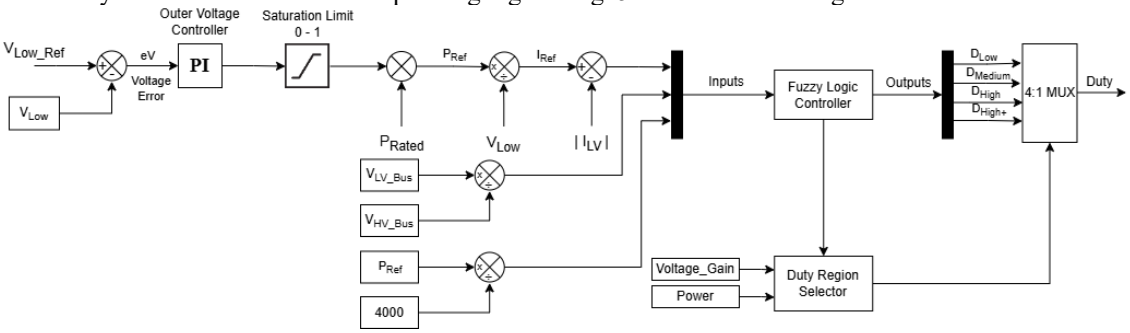


Fig. 5. PI-assisted fuzzy control structure.

Table 2. Fuzzy-controller inputs and duty-region selection.
(a) Membership-function configuration

Variable	Range	Sets	Shape
Current error	$[-0.5, 0.5]$	5	Triangular; linear edges
Voltage-gain input	$[0.3, 0.7]$	3	Triangular; linear edges
Power reference	$[0.5, 1.0]$	3	π-type center; linear edges
Duty regions	R_1–R_4	5/5/5/6	Triangular; linear edges

(b) Duty region versus nominal voltage pair and power

Voltage pair (V)	2 kW	3 kW	4 kW
400–800	R_3	R_4	R_4
400–1200	R_2	R_3	R_3
800–1200	R_1	R_1	R_2

R_1: $0.07 \le D \le 0.10$; R_2: $0.12 \le D \le 0.21$;
R_3: $0.23 \le D \le 0.34$; R_4: $0.38 \le D \le 0.49$.

V. SIMULATION RESULTS

CASCADED PI CONTROL SIMULATION RESULTS

Fig. 6 presents the MATLAB/Simulink implementation of the proposed converter with cascaded PI control. The battery interfaces, six-switch power stage, energy-storage and leakage inductances, transformer, and DC-link capacitors are shown at the main model level. Separate subsystems implement the cascaded PI algorithm, pre-charge supervision, and SoC-based gate-signal assignment. The controller subsystem receives the voltage reference, measured battery and bus variables, power-reference information, and operating-mode flag, and generates the gate signals for S1–S2. The pre-charge subsystem processes battery- and bus-voltage measurements to generate the pre-charge and bypass commands, together with the converter-enable signal. The SoC-based subsystem supplies the switching signals for S3–S6 and the mode flag used by the cascaded controller. Within the controller subsystem, the outer voltage PI loop determines the power demand and corresponding current reference, while the inner PI loop regulates the battery-current magnitude through the auxiliary duty cycle, following the control structure in Fig. 4.

The converter is evaluated at a switching frequency of 100 kHz using the component values listed in Table 1. The nominal voltage-transfer conditions are 1200 → 800 V and 1200 → 400 V for step-down operation, and 800 → 1200 V and 400 → 1200 V for step-up operation. For the selected transfer direction, the source and receiving batteries are initialized at 80% and 30% SoC, respectively. The operating cases are identified by their nominal battery voltages, while the plotted waveforms show the simulated terminal voltages and port currents. Full-load operation is assessed at the 4 kW reference, and transitions from 4 to 2 kW are used to evaluate the response to a reduced power command. The assessment considers average input and output powers, conversion efficiency, receiving-port current magnitude and RMS value, RMS current ripple, and settling time. The receiving port is the low-voltage battery during step-down operation and the high-voltage battery during step-up operation. The same converter parameters and nominal operating conditions are used for the subsequent comparison with PI-assisted fuzzy control.

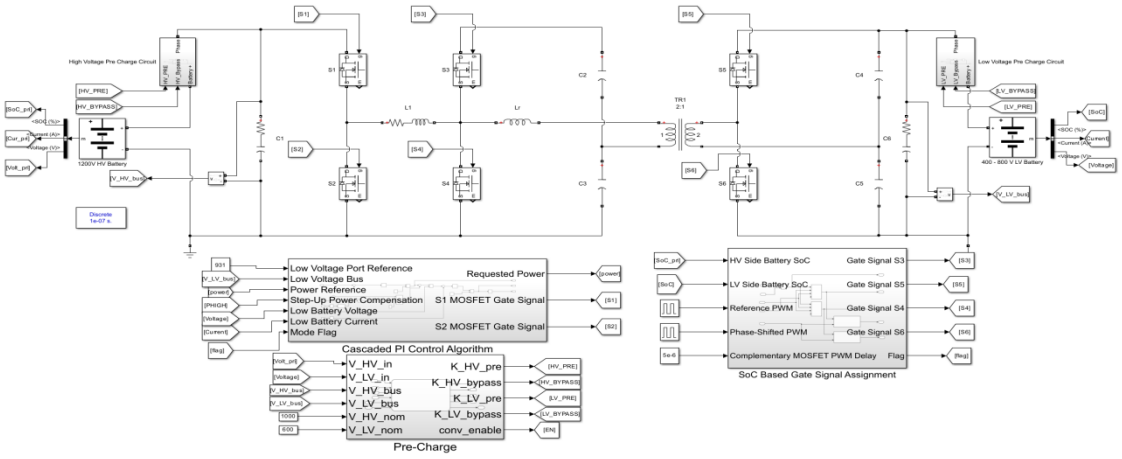


Fig. 6. Cascaded PI Controller Simulation in MATLAB/Simulink

Step-down operation

Fig. 7(a–b) shows periodic source- and receiving-port waveforms at approximately 1297 and 856 V. Receiving-current mean magnitude and RMS value are 4.648 and 4.763 A, with 1.0 A RMS ripple. The average output power is 3.972 kW, yielding 94.21% simulated efficiency, −0.70% output-power error, and a 0.67 s full-load settling time.

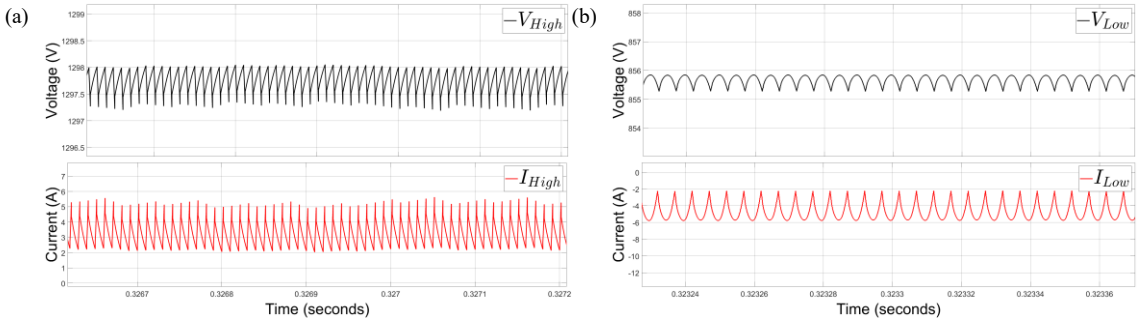


Fig. 7. Cascaded-PI source- and receiving-port waveforms for 1200 → 800 V operation: (a) source port and (b) receiving port.

Fig. 8(a) shows the high-voltage source waveforms. Fig. 8(b) records a 428.5 V receiving port, mean and RMS currents of 9.356 and 9.461 A, and 1.4 A RMS ripple.

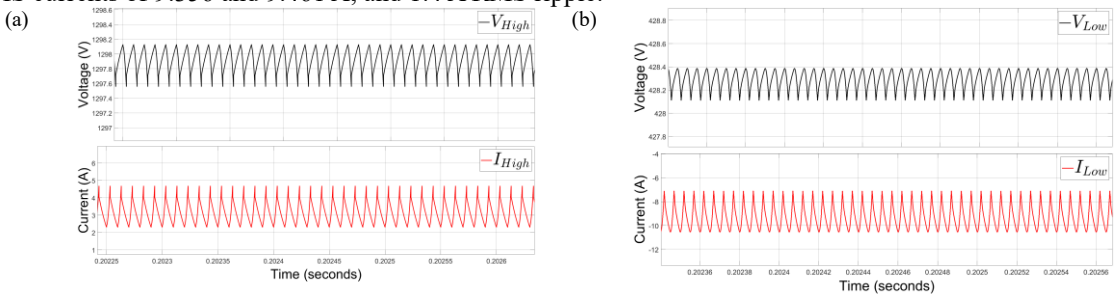


Fig. 8. Cascaded-PI source- and receiving-port waveforms for 1200 → 400 V operation: (a) source port and (b) receiving port.

Step-up operation

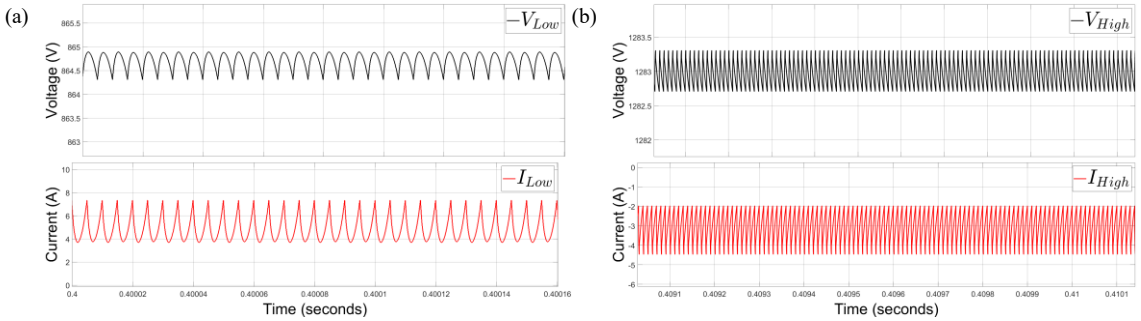


Fig. 9. Cascaded-PI source- and receiving-port waveforms for 800 → 1200 V operation: (a) source port and (b) receiving port.

Fig. 9(a–b) records source and receiving voltages of approximately 864.5 and 1283 V. Receiving-current mean magnitude and RMS value are 3.090 and 3.179 A, with 0.7 A RMS ripple. At this operating point, the average input and output powers are 4.460 and 4.040 kW, respectively, corresponding to 90.58% simulated efficiency and a +1.00% output-power error. The full-load settling time is 0.89 s. The positive source current and negative receiving current in Fig. 9 reflect the adopted port-current convention: the low-voltage battery supplies energy, while the high-voltage battery receives it.

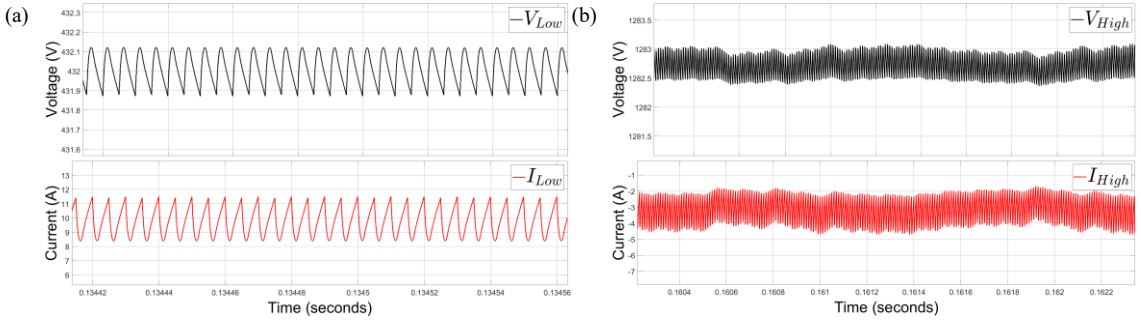


Fig. 10. Cascaded-PI source- and receiving-port waveforms for 400 → 1200 V operation: (a) source port and (b) receiving port.

Fig. 10(a–b) shows a 431.5 V source and 1283 V receiving port. Receiving-current mean magnitude and RMS value are 3.211 and 3.293 A, with 0.7 A RMS ripple.

PI-ASSISTED FUZZY CONTROL SIMULATION RESULTS

Fig. 11 presents the MATLAB/Simulink implementation with PI-assisted fuzzy control. The controller, duty-region selector, pre-charge supervision, and SoC-based gate-signal assignment are organized as separate subsystems connected to the battery interfaces and converter power stage. Within the controller subsystem, the outer voltage PI loop generates the power demand and current reference, while fuzzy inference adjusts the auxiliary duty command according to the current error. The voltage-gain and power inputs determine the admissible duty region through the separate selector subsystem, following the control structure in Fig. 5 and the region definitions in Table 2. The step-down tests cover the nominal 1200 → 800 V and 1200 → 400 V transfer conditions at power references of 2 and 4 kW. The source and receiving batteries are initialized at 80% and 30% SoC, respectively, using the same converter parameters as in the cascaded PI cases. For 1200 → 800 V operation, regions R_1 and R_2 are selected at 2 and 4 kW, respectively; the corresponding 1200 → 400 V cases use regions R_2 and R_3. The following results present the full-load voltage and current waveforms and compare the responses of both controllers to the subsequent reduction in the power reference from 4 to 2 kW.

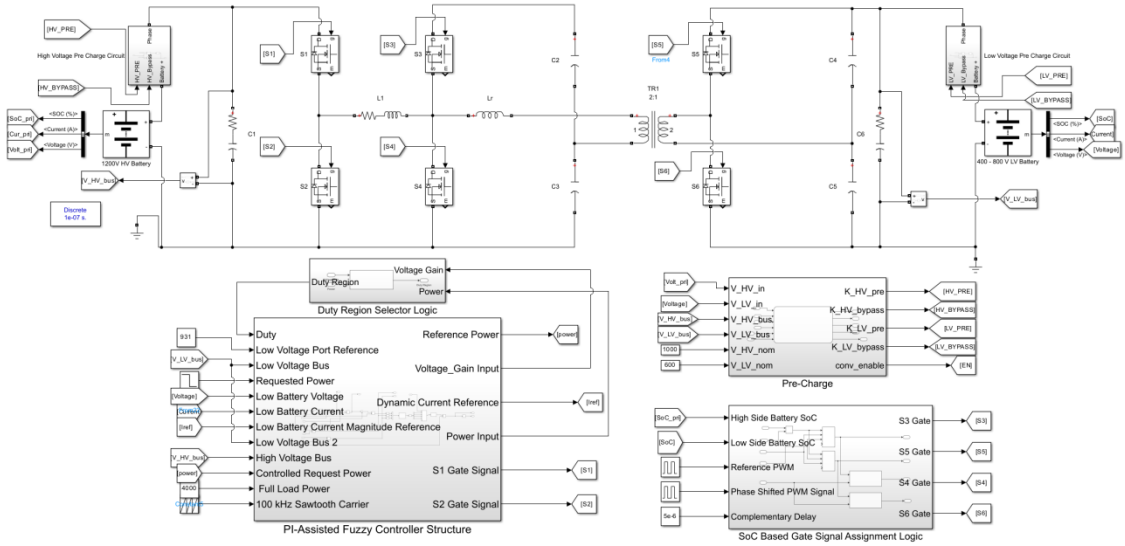


Fig. 11. MATLAB/Simulink implementation with PI-assisted fuzzy control.

Step-down operation

Fig. 12(a–b) presents the source- and receiving-port voltage and current waveforms under PI-assisted fuzzy control for the 1200 → 800 V transfer condition. The receiving-current mean magnitude and RMS value are 4.605 and 4.730 A, with an RMS ripple component of 1.1 A. The average input and output powers are 4.140 and 3.950 kW, respectively, corresponding to 95.41% simulated efficiency and a −1.25% output-power error relative to the 4 kW reference. Fig. 13 compares the responses of both controllers to the subsequent reduction in the power reference from 4 to 2 kW.

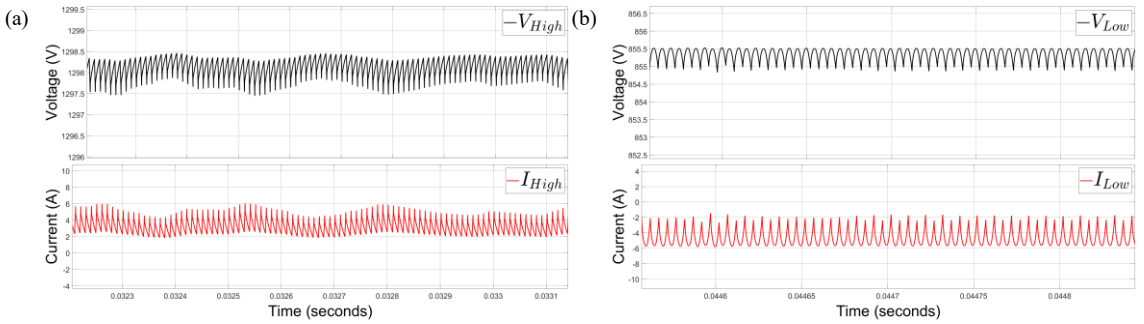


Fig. 12. PI-assisted-fuzzy source- and receiving-port waveforms for 1200 → 800 V operation: (a) source port and (b) receiving port.

In Fig. 13, both controllers follow the 4-to-2 kW step and reach a bounded reduced-power region. Cascaded PI requires approximately 0.65 s; fuzzy control completes the principal adjustment within a few milliseconds. The receiving-port RMS current ripple is 1.1 A, compared with 1.0 A for cascaded PI, showing that the faster response does not entail a reduction in steady-state current ripple.

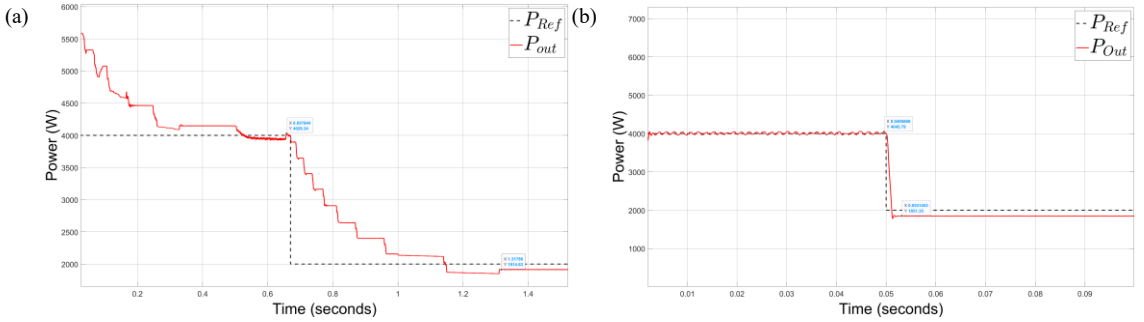


Fig. 13. Full-to-half-load power response at 1200 → 800 V: (a) cascaded PI control and (b) PI-assisted fuzzy control.

Fig. 14(a–b) presents the source and receiving waveforms. At the 428 V receiving port, mean and RMS currents are 9.432 and 9.516 A, with 1.3 A RMS ripple. The high-voltage bus and source-current waveforms remain bounded and periodic throughout the displayed interval, with no visible sustained drift at the widest investigated step-down ratio.

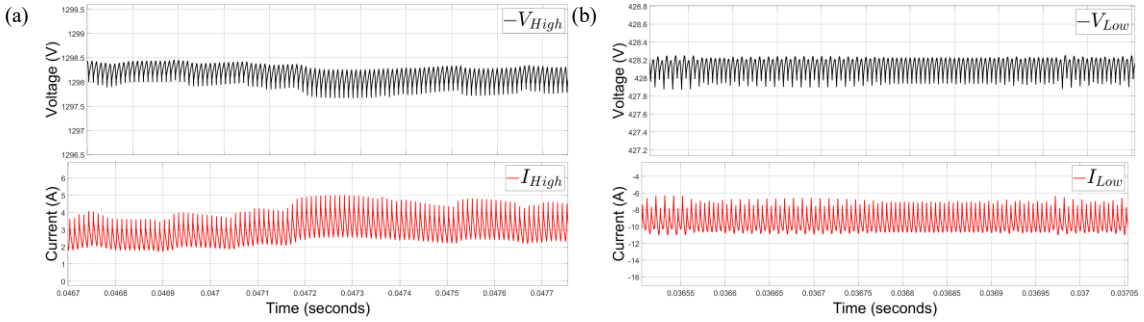


Fig. 14. PI-assisted-fuzzy source- and receiving-port waveforms for 1200 → 400 V operation: (a) source port and (b) receiving port.

At this voltage-transfer condition, the average input and output powers are 4.120 and 4.040 kW, respectively, giving 98.06% simulated efficiency and a +1.00% output-power error. The full-load settling time is 8 ms, compared with 0.65 s for cascaded PI. The mean receiving current is approximately twice that at the 1200-to-800 V operating point, consistent with transferring a similar power level at approximately half the receiving-port voltage.

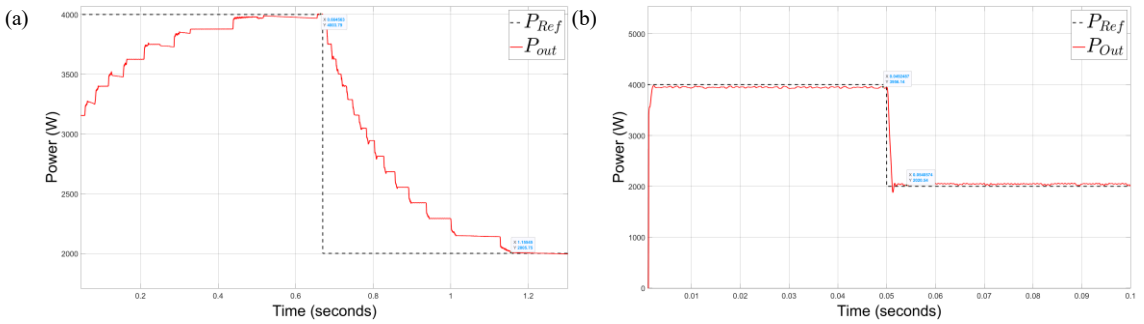


Fig. 15. Full-to-half-load power response at 1200 → 400 V: (a) cascaded PI control and (b) PI-assisted fuzzy control.

Fig. 15 shows bounded recovery near the 2 kW command with low residual ripple. PI adjustment occurs on a sub-second scale; the fuzzy response completes its dominant adjustment within a few milliseconds.

Step-up operation

Reverse transfer tests cover 800 → 1200 V and 400 → 1200 V at 2 and 4 kW, with initial source and receiving SoCs of 80% and 30%. The 800–1200 V cases use R_1 and R_2; 400–1200 V uses R_2 and R_3 at 2 and 4 kW, respectively.

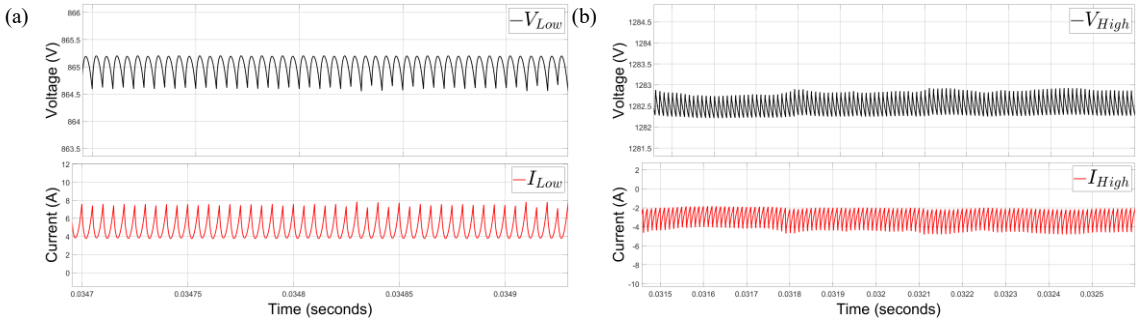


Fig. 16. PI-assisted-fuzzy source- and receiving-port waveforms for 800 → 1200 V operation: (a) source port and (b) receiving port.

Fig. 16(a–b) shows periodic source and receiving waveforms at approximately 865 and 1283 V. Receiving-current mean magnitude and RMS value are 3.105 and 3.187 A, with 0.7 A RMS ripple.

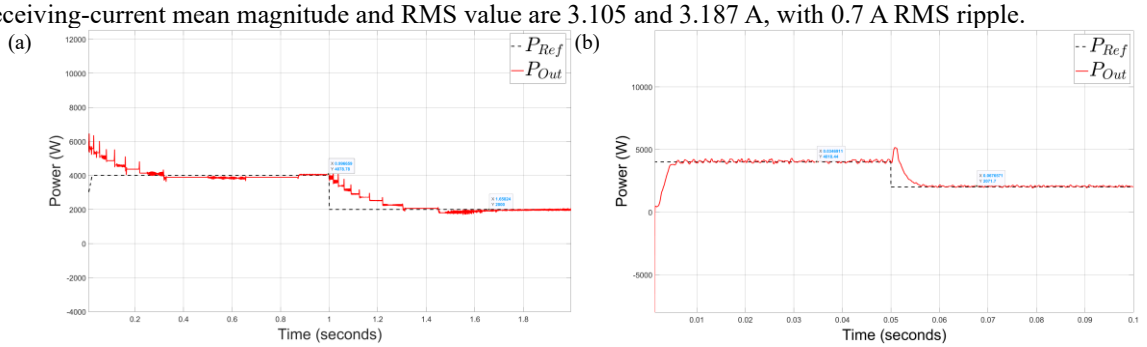


Fig. 17. Full-to-half-load power response at 800 → 1200 V: (a) cascaded PI control and (b) PI-assisted fuzzy control.

In Fig. 17, both controllers recover after the reference step. Fuzzy control reaches the reduced-power region within several milliseconds, with a brief overshoot; PI recovery is more gradual. Both subsequently remain bounded near the command.

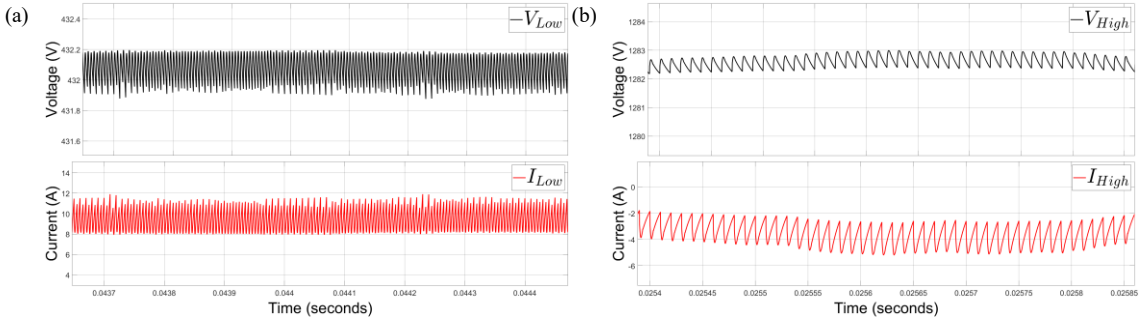


Fig. 18. PI-assisted-fuzzy source- and receiving-port waveforms for 400 → 1200 V operation: (a) source port and (b) receiving port.

Fig. 18(a–b) shows bounded periodic waveforms at approximately 432 and 1283 V for the largest step-up ratio. Receiving-current mean magnitude and RMS value are 3.087 and 3.362 A, with 1.3 A RMS ripple. Fig. 19 shows recovery toward 2 kW at 400 → 1200 V. Fuzzy control completes the principal adjustment in the millisecond range; cascaded PI evolves more gradually.

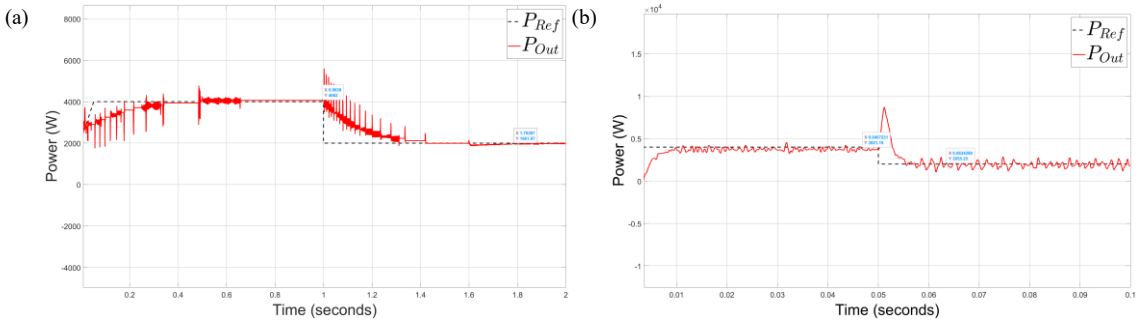


Fig. 19. Full-to-half-load power response at 400 → 1200 V: (a) cascaded PI control and (b) PI-assisted fuzzy control.

The full-load and transient results demonstrate closed-loop transfer in both directions across the four conditions. Table 3 summarizes the eight full-load operating points.

Table 3. Full-load simulation metrics. e_P is the signed output-power error relative to the 4 kW reference, t_s is the full-load settling time, and ΔI_{rms} is the receiving-port RMS current ripple.

Control	Transfer (V)	P_{in} (kW)	P_{out} (kW)	η (%)	e_P (%)	t_s (s)	ΔI_{rms} (A)
PI	1200 → 800	4.216	3.972	94.21	−0.70	0.67	1.0
PI	1200 → 400	4.110	4.000	97.32	0.00	0.65	1.4
PI	800 → 1200	4.460	4.040	90.58	+1.00	0.89	0.7
PI	400 → 1200	4.486	4.062	90.55	+1.55	0.66	0.7
Fuzzy	1200 → 800	4.140	3.950	95.41	−1.25	0.006	1.1
Fuzzy	1200 → 400	4.120	4.040	98.06	+1.00	0.008	1.3
Fuzzy	800 → 1200	4.320	4.050	93.75	+1.25	0.007	0.7
Fuzzy	400 → 1200	4.160	3.940	94.71	−1.50	0.012	1.3

VI. DISCUSSION

The full-load results in Table 3 show that the proposed converter achieves bidirectional power transfer over the investigated battery-voltage range. Both controllers regulate power close to the rated level, and the simulated waveforms remain bounded in steady state. The power-flow direction and voltage-conversion ratio influence the current distribution, simulated efficiency, and transient behavior. The cascaded PI controller offers a simple and predictable structure that maintains stable power regulation after the initial transient. Its settling times (0.65–0.89 s) are longer than those of the PI-assisted fuzzy controller, but its power traces are smoother, making it a suitable baseline. Overall, the cascaded PI controller provides a simple and robust baseline with predictable steady-state behavior, whereas the PI-assisted fuzzy controller provides a substantially faster dynamic response. The main advantage of the fuzzy controller is its rapid adjustment of the converter power, while its main limitation is the greater sensitivity of the transient response to controller tuning.

VII. CONCLUSION

This paper presented the design, analysis, and validation of a high-voltage cascaded bidirectional DC/DC converter tailored for vehicle-to-vehicle (V2V) charging applications. By integrating a bidirectional buck–boost stage with a dual active half-bridge (DAHB) converter, the architecture achieves wide-range, galvanically isolated, and bidirectional power transfer. The theoretical foundation was established through a detailed analysis of the step-down operating principle, steady-state voltage gain, power-transfer characteristics, component selection criteria, and a hybrid modulation strategy. Furthermore, two distinct closed-loop control frameworks were developed and evaluated under identical operating parameters. MATLAB/Simulink program validated the stable performance of the topology across both step-down and step-up modes. Comparative assessments demonstrated that while the cascaded PI controller offers simplicity and stable steady-state regulation, the PI-assisted fuzzy controller significantly enhances dynamic performance during abrupt load-demand variations. Specifically, the fuzzy-based strategy yields faster power tracking and a reduced transient response time. Ultimately, the theoretical and simulation findings confirm that the developed cascaded topology and PI-assisted fuzzy control strategy provide a highly suitable, robust solution for high-voltage, wide-voltage-range, and dynamic V2V charging infrastructures.

AUTHOR DECLARATIONS

Conflict of Interest—The authors declare that they have no conflicts of interest with any person or organization.
Ethics Committee Approval—Ethics committee approval is not required for this article.
Use of Artificial Intelligence Tools—ChatGPT was used for grammar and spell checking.

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