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Three-Phase, Four-Wire UPQC Topology with Reduced Switching Losses

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Abstract: The paper introduces the modified UPQC topology with reduced switching losses. UPQC is a versatile custom power device which consists of two inverters connected back to back and deals with both load current and supply voltage imperfections. It can simultaneously perform as shunt and series active power filters. The series part of the UPQC acts as Dynamic Voltage Restorer (DVR). It is used to maintain balanced, distortion free nominal voltage at the load. The shunt part of the UPQC acts as Distribution STATIC Compensator (DSTATCOM) and it is used to compensate load reactive power, harmonics and balance the load currents there by making the source current balanced and distortion free with unity power factor. The efficiency of the proposed configuration has been verified through simulation using MATLAB/SIMULINK

Keywords*: Static VAR Compensator (SVC), voltage source converter (VSC), Dynamic Voltage Restorer (DVR*)

I. INTRODUCTION

In this paper, a modified Unified power quality conditioner (UPQC) topology for three-phase four-wire system was used and it has the capability to compensate the load at a lower dc-link voltage under non stiff source. Design of the filter parameters for the series and shunt active filters.In general, with the advancement of power electronics and digital control technology, the renewable energy sources are increasingly being connected to the distribution systems. In the power distribution network the power quality has degraded due to nonlinear loads and unbalanced loads.So, in this paper, the power distribution has a voltage and a current-related PQ issue was reduced by using custom power device of Unified power quality conditioner (UPQC). This topology enables UPQC to have a reduced dc-link voltage without compromising its compensation capability. This topology also helps to match the dc-link voltage requirement of the shunt and series active filters of the UPQC.

The topology uses a capacitor in series with the interfacing inductor of the shunt active filter, and the system neutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourth leg in the voltage source inverter (VSI) of the shunt active filter.

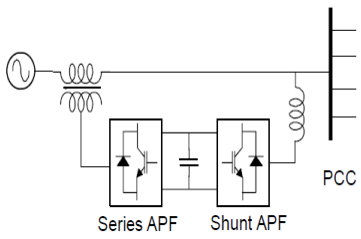


Fig. 1: Hard ware structure of UPQC

The average switching frequency of the switches in the VSI also reduces; consequently the switching losses in the inverters reduce. In existing system the three phase three WIRE UPQC has used. Mainly Voltage rating of dc-link capacitor largely influences the compensation performance of an active filter. So the dc-link voltage for the shunt active filter has much higher value than the peak value of the line-to-neutral voltage. In this method the UPQC which requires more rating of series and shunt active filters. Additionally to maintain the Low harmonics level by adding passive filters. Further, in this topology, the system neutral is connected to the negative terminal of the dc bus. This will avoid the requirement of the fourth leg in VSI of the shunt active filter and enables Independent control of each leg of the shunt VSI with single dc capacitor.The current paper presents a novel control strategy of a three-phase, four-wire Unified Power Quality (UPQC) to improve power quality. The UPQC is realized by the integration of series and shunt active power filters (APF) sharing a common dc bus capacitor. The realization of shunt APF is carried out using a three-phase, four-leg Voltage Source Inverter (VSI), and the series APF is realized using a three-phase, three-leg VSI. To extract the fundamental source voltages as reference signals for series APF, a zero-crossing detector and sample-and-hold circuits are used. For

the control of shunt APF, a simple scheme based on the real component of fundamental load current (I CosΦ) with reduced numbers of current sensors is applied.

II. CONVENTIONAL AND PROPOSED TOPOLOGIES OF UPQC

In this section, the conventional and proposed topology of the UPQC is discussed. Fig. 2 shows the power circuit of the neutral-clamped VSI topology-based UPQC. This topology requires two dc storage devices, each leg of the VSI can be controlled independently, and tracking is very smooth with less number of switches when compared to other VSI topologies [1]. In this figure, v_{sa}, v_{sb}, and v_{sc} are source voltages of phases *a*, *b*, and *c*, respectively. Similarly, v_{ta}, v_{tb}, and v_{tc} are terminal voltages. The series active filter voltages are represented by v_{dvra}, v_{dvrb}, and v_{dvrc}.The three phase source currents are represented by i_{sa}, i_{sb} and i_{sc}. i_{la}, i_{lb} and i_{lc} are represented for load currents.

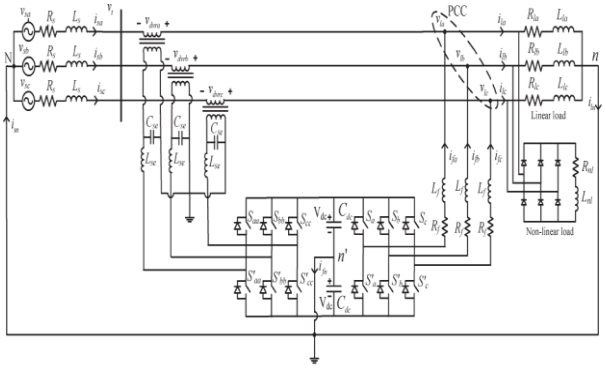


Fig.2: Power circuit of neutral-clamped VSI topology-based UPQC

The shunt active filter currents are represented by i_{fa}, i_{fb}, i_{fc} and current in the neutral leg is denoted by i_{ln}. The feeder inductance is denoted by Ls and the feeder resistance denoted by R_s respectively. The interfacing inductance of shunt active filter is denoted by L_f and resistance of the shunt active filter represented by R_f respectively, and the interfacing inductance of the series active filter denoted by L_{se}, the filter capacitor of the series active filter represented by C_{se} respectively. The linear and nonlinear loads as shown in this figure. The dc-link capacitors and voltages across them are denoted by $C_{dc1} = C_{dc2} = C_{dc}$ and $V_{dc1} = V_{dc2} = V_{dc}$, respectively, and V_{dbus} ($V_{dc1} + V_{dc2} = 2V_{dc}$) is the total dc-link voltage. In this conventional topology, the voltage across each common dc-link capacitor is taken as 1.6 times the peak value of the source voltages.

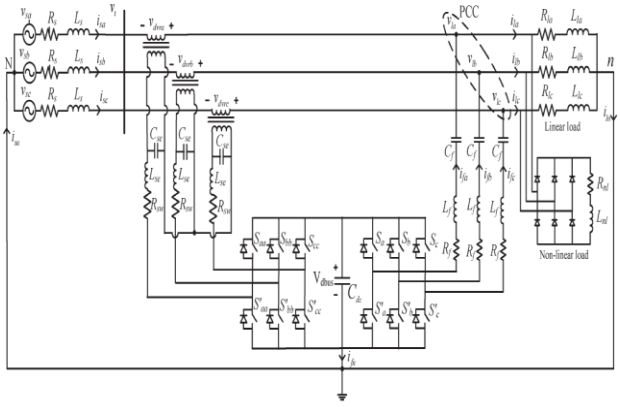
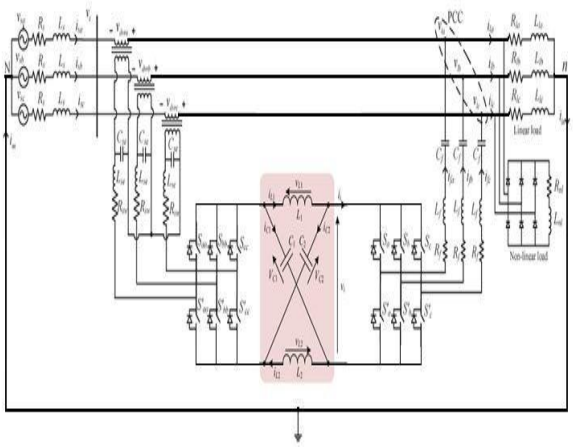


Fig.3: Equivalent circuit of proposed VSI topology for UPQC compensated system

Fig. 3 shows the equivalent circuit of the proposed VSI topology for UPQC compensated system. In this modified topology, the system neutral has been connected to the negative terminal of the dc bus along with the capacitor C_f in series with the interfacing inductance of the shunt active filter. This topology is referred to as modified topology. The capacitor C_f has the capability to supply a part of the reactive power required by the load, and the active filter is capable of doing two functions. Compensating the load harmonics and balanced reactive power is compensated. The compensated performance is affected by the design of capacitor C_f and other VSI parameters. This modified topology uses a single dc capacitor with negative terminal connected to

ground, in order to avoid fourth leg in shunt active filter; also the single capacitor does not required dc-link voltage balancing. Unlike the topologies mentioned in the literature [2], [3], [4], [5], in the shunt active filter, the independent control of each leg can be achieved. In neutral clamped topology, independent control is possible when dc link voltage balance occurs. In fourth leg VSI topology, the dc-link voltage balance occur but independent control is not possible The performance of this topology will be explained in detailed in the following section.



4: Equivalent circuit of proposed Z-source topology for UPQC

III. DESIGN OF VSI PARAMETERS

The VSI parameters are V_{dc}, C_{dc}, L_f , L_{se}, C_{se}, and switching frequency (f_{sw}). The design details of the VSI parameters for the shunt and series active filter are given in [6], [7]. Based on the following equations.

A. Design of Shunt Active Filter VSI Parameters

Consider the active filter is connected to an X kVA system and deals with 0.5X kVA and 2X kVA handling capability under transient conditions for *n* cycles. During transient, with an increase in system kVA load, the voltage across each dc-link capacitor (V_{dc}) decreases and vice versa. Allowing a maximum of 25% variation in V_{dc} during transient, the differential energy (ΔE_c) across C_{dc} is given by

$$\Delta E_c = \frac{C_{dc}[(1.25V_{dc})^2-(0.875V_{dc})^2}{2} \quad (1)$$

The change in system energy (ΔE_s) for a load change from 2X kVA to 0.5X kVA is

$$\Delta E_s = (2X - X/2)\, nT. \quad (2)$$

Where, V_m is the peak value of the source voltage, X is the kVA rating of the system, n is number of cycles, and T time period of each cycle. $V_{dc} = mV_m$, and it is found that $m = 1.6$. The approximate relationship between *minimum* switching frequency (f_{swmin}) ,and maximum switching frequency (f_{swmax}).

$$m = \frac{1}{\sqrt{1-f_{swmin}\ /f_{swmax}}} \quad (3)$$

,,

Based on this, the shunt interfacing inductance has been derived taking in to consideration of the maximum switching frequency and is given below

$$L_f = \frac{mV_m}{4h_1 f_{swmax}} \quad (4)$$

$$h_1 = \sqrt{\frac{k_1}{k_2}\frac{(2m^2-1)}{4m^2} f_{\mathrm{swmax}}}$$

Where, $h1$ is the hysteresis band limit, $k1$ and $k2$ are proportionality constants.

B. Design of Series Active Filter VSI Parameters

In order to make the series active filter system a first-order system, a resistor is added in series with the filter capacitor, referred as switching band resistor (R_{sw}). The rms value of the capacitor current can be expressed as

$$I_{se} = \sqrt{I_{inv}^2 - I_l^2} \quad (5)$$

I_{inv} is the series inverter current rating and I_l is the load current[9]. The capacitor branch current is divided into two components-a fundamental current I_{se1}, corresponding to the fundamental reference voltage (V_{ref1}) and a switching frequency current *I*sw, corresponding to the band voltage (V_{sw}). The DVR voltage and the current of the capacitor are given by

$$V_{dvr} = \sqrt{V_{ref1}^2 + V_{sw}^2}$$

$$I_{se} = \sqrt{I_{se1}^2 + I_{sw}^2} \qquad (6)$$

The resistance (R_{sw}) and the capacitance (C_{se}) values are expressed in terms of band voltage *v*sw and rated references voltage (V_{ref1}), respectively, and are given by

$$R_{sw} = \frac{h_2}{I_{sw}\sqrt{3}}$$

$$C_{se} = \frac{I_{se1}}{V_{ref1} 2\pi f_1} \qquad (7)$$

The interfacing inductor L_{se} has been designed based on the switching frequency of the series active filter and is given by

$$L_{se} = \frac{(V_{bus})R_{sw}}{4 f_{swmax}\ h_2} \qquad (8)$$

Where V_{bus} is the total dc-link voltage across both the dc-link capacitors.

The line to neutral rated voltage is 230V and the dc-link voltage reference (V_{dcref}) of the conventional VSI topology has been taken as 1.6 V_m for each capacitor. The hysteresis band ($h1$) is taken as 0.5 A. From (4), the interfacing inductance (Lf) is computed to be 26mH. The base kVA rating of the system is taken as 5kVA. Using (3), C_{dc} is computed and found to be 2200μF. The rated series VSI voltage is chosen as 50% of the rated voltage, i.e., the maximun injection capacity of the series active filter is 115 V. The hysteresis band ($h2$) for series active filter is taken as 3% of the rated voltage, i.e., 6.9 V. The maximum switching frequency of the IGBT-based inverter is taken as 10 kHz. The series active filter current rating is choosen as 8 A and the rated load current as 7 A. Using the (7)– (9), the filter capacitor C_{se}, the band resistor R_{sw} and interfacing inductance L_{se} are calculated to be 80 μF, 1.5 Ω, and 5 mH, respectively[10].

IV. GENERATION OF REFERENCE COMPENSATOR CURRENTS UNDER UNBALANCED AND DISTORTED VOLTAGES

In this work, the load currents are unbalanced and distorted, these currents flow through the feeder impedance and make the voltage at terminal unbalanced and distorted. The series active filter makes the voltages at PCC balanced and sinusoidal. However, the voltages still contain switching frequency components and they contain some distortions. If these terminal voltages are used for generating the shunt filter current references, the shunt algorithm results in erroneous compensation [11].

To remove this limitation of the algorithm, fundamental positive sequence voltages $v+ la1\ (t)$, $v+ lb1\ (t)$, and $v+ lc1\ (t)$ of the PCC voltages are extracted and are used in control algorithm for shunt active filter. The expressions for reference compensator currents are given in (7). In this equation, *Pl*avg is the average load power, *P*loss denotes the switching losses and ohmic losses in actual compensator, and it is generated using a capacitor voltage PI controller. The term *Pl*avg is obtained using a moving average filter of one cycle window of time *T* in seconds. The term ϕ is the desired phase angle between the source voltage and current [12]

$$i_{fa}^* = i_{la} - i_{sa}^* = i_{la} - \frac{v_{la1}^+ + \gamma\left(v_{lb1}^+ - v_{lc1}^+\right)}{\Delta_1^+}\left(P_{lavg} + P_{loss}\right)$$

$$i_{fb}^* = i_{lb} - i_{sb}^* = i_{lb} - \frac{v_{lb1}^+ + \gamma\left(v_{lc1}^+ - v_{la1}^+\right)}{\Delta_1^+}\left(P_{lavg} + P_{loss}\right)$$

$$i_{fc}^* = i_{lc} - i_{sc}^* = i_{lc} - \frac{v_{lc1}^+ + \gamma\left(v_{la1}^+ - v_{lb1}^+\right)}{\Delta_1^+}\left(P_{lavg} + P_{loss}\right)$$

Where,

$$\Delta = \sum_{j=a,b,c}\left(v_{lj1}^+\right)^2, \gamma = \tan\varphi / \sqrt{3}.$$

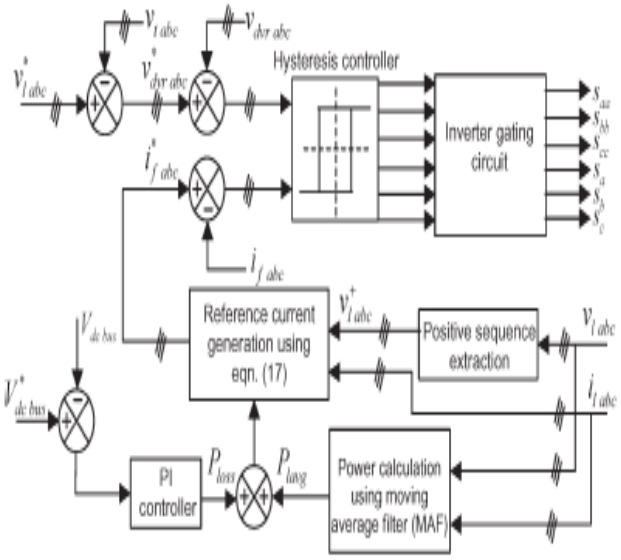
The above algorithm gives balanced source currents after compensation irrespective of unbalanced and distorted supply. The reference voltages for series active filter are given as

$$v^*_{dvri} = v^*_{li} - v_{ti}$$

$$i = a, b, c$$

Where v^*_{li} represents the desired load voltages in three phases, and v^*_{dvri} represents the reference series active filter voltages.

Fig.5: Control block diagram for UPQC



ADVANTAGES:

- The reactive power is injected along with the sinusoidal current,
- The voltage and current regulation is done effectively,
- The Power factor is maintained even if the load is varied [13].

APPLICATIONS:

- Distribution Generation (DG systems)
- Grid Control Systems
- Transmission Lines [14].

IV. SIMULATION RESULT

The simulation results of the new topology was simulated with the mat lab and the simulated results are given below

Fig.6: Shows the voltage across both dc capacitors .these are maintained constant.
Fig.7: Shows the Inverter output voltage in leg-a of shunt active filter.
Fig.8: Shows the simulation results before compensation loads.
Fig.9: Shows the terminal voltages with sag, DVR- injected voltages, and load voltages after compensation.
Fig.10: Shows the shunt active filter currents.

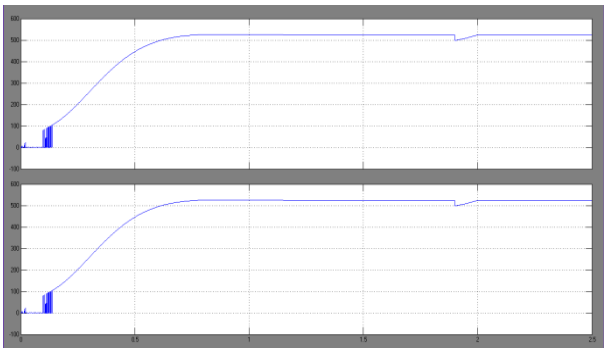


Fig. 6: Shows the DC and fundamental values of voltage across series capacitor and inverter output voltage

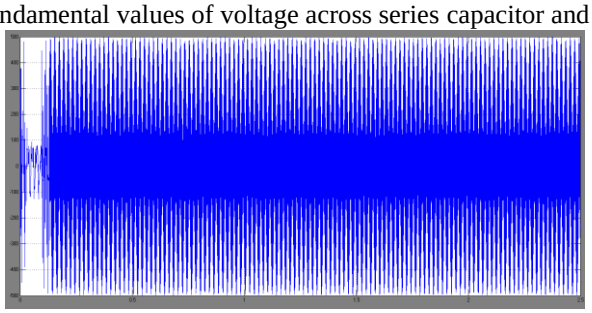


Fig. 7: Shows the Inverter output voltage in leg-aOf shunt active filter

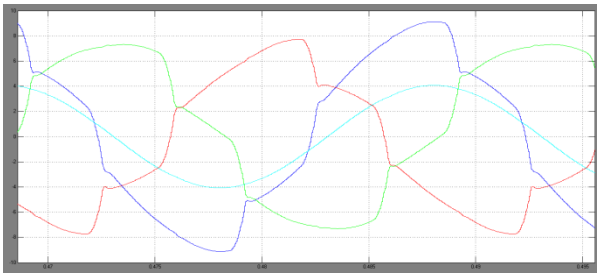


Fig.8: Shows the simulation results before compensation load currents

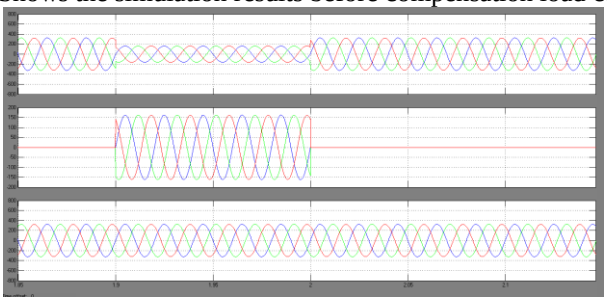


Fig. 9: Shows the Terminal voltages with sag, DVR-injected voltages and load voltages after compensation

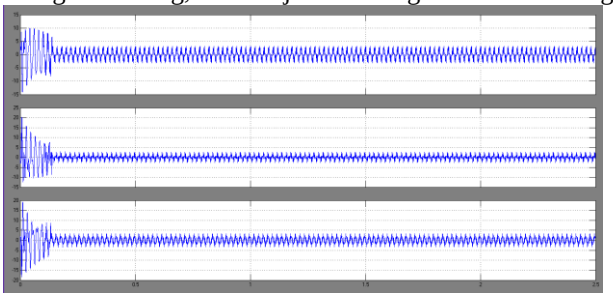


Fig.10: Shows the Shunt active filter currents.

V. CONCLUSION

A modified UPQC topology for three-phase four-wire system has been proposed in this paper. The proposed method is validated through simulation in a three-phase distribution system with neutral-clamped UPQC topology (conventional). The proposed modified topology gives the advantages of both the conventional neutral-clamped topology and the four-leg topology. In this paper found that the modified topology has less average switching frequency, and less THDs in the source currents, and load voltages with reduced dc-link voltage as compared to the conventional UPQC topology.

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