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Systematic Design of Hybrid Cascaded Multilevel Inverters with Simplified DC Power Supply and low Switching Losses

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Abstract: *Hybrid cascade multilevel inverters combine semi conductor devices of different voltage ratings and technologies which theoretically allow high efficiency to be achieved. The bottlenecks of these topologies are, however, the need for isolated supplies for the cells and the lack of modularity. This paper focuses on the design and control of high-resolution, high-efficiency multi level inverters with simplified dc power supplies. for which all unsupplied capacitor voltages can be regulated Six classes of inverters are obtained covering single- and three phase ,staircase and pulse width-modulated (PWM) inverters. New configurations of hybrid cascade multilevel inverters are obtained for each class. A double modulation strategy with two different frequencies is proposed that allows switching losses of PWM inverters to be reduced. Decoupled mechanisms are proposed for the total and internal energy balances. An analysis of the maximum voltage utilization and efficiency of the resulting configurations is carried out.*

Index Terms: *AC-DC power converters, asymmetrical multilevel inverters, cascade multilevel inverters, hybrid multilevel inverters ,multilevel converters, multilevel topologies, pulse width modulation converters, series connected converters.*

I.INTRODUCTION

Multilevel inverters have attracted interest for increasing the operating voltage of power conversion devices far beyond the blocking voltage of single switching devices and also for reducing the distortion of the waveforms applied to the load. Among the available topologies cascade multilevel inverters are conceptually the simplest as they combine standard H-bridge inverters in series. Hybrid asymmetrical cascade multilevel inverters however present many challenges as they combine cells of different voltage ratings different topologies or even combine switch converters with linear amplifiers. The main idea behind the hybrid asymmetrical cascade inverter concept is to obtain a better inverter by hybridizing the properties of several cells and switches. In particular, the combination of slow switches, featuring high blocking voltage capabilities and low relative conduction losses, with fast switches, featuring low switching losses aims at obtaining a hybrid inverter with better equivalent switches that would feature fast switching capability, low conduction losses, and low switching losses. By operating the high-voltage cells at reduced switching frequency, far below the pulse width modulation (PWM) frequency performing the PWM only with the low-voltage cells, the conversion losses of the inverter *alone* can indeed be reduced.

The main property supporting this result is that the transitions between most pairs of levels involve only the transition of the low-voltage cell. This cannot however be achieved for all topologies for all operating points. By designing and controlling the inverter appropriately, it is, however, possible to modulate all pairs of adjacent levels by switching only the low-voltage cells. It has to be noted that the ideas formerly developed in for quasi linear amplifiers are conceptually very similar and mathematically yield exactly the same design and control strategies. The concepts for obtaining reduced switching losses have been optimized and generalized for single-phase inverters by the introduction of optimized transition graphs in the switching-state space and for three-phase inverters by introducing the concept of modulation domain.

The bottlenecks that still prevent the deployment of these topologies for industry applications are as follows:

1) The need for isolated supplies for all cells, which increases the complexity, cost, and losses of the inverter;
2) the difficulty of designing and controlling topologies with simplified supplies. This increases the complexity of the control and reduces the maximum voltage utilization of the inverter. As it is not possible to use the full inverter voltage, it is necessary to augment the blocking voltage capability of the inverter, which results in

augmented cost and reduced energy efficiency;
3) the lack of modularity. The supply issues have attracted the attention of many researchers. Rech and Pin heiro derived design rules for canceling *passively* the circulation of power between the cells, in order to allow the supply with only rectifiers. Mari´ethoz and Rufer proposed an efficient multisource dc–dc converter to reduce supply losses .Du *et al.* investigated how to apply programmed PWM in the context of partially supplied inverter. Lu and Corzine proposed the use of a topology where a motor load serves as isolation between the dc links of two NPC inverters. Steimer and Manjrekar proposed a topology that combines three-phase neutral point clamped (NPC) with unsupplied filtering floating H-bridge cells.

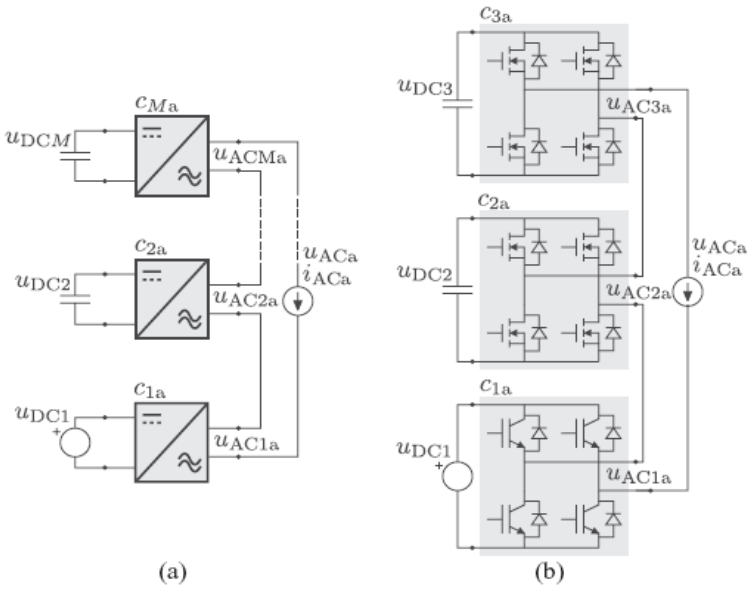


Fig.1. Investigated single-phase inverter topologies combine cells with different supply voltages and switch devices voltages (a) and technologies (b). (a) General single-phase topology. (b) Asymmetrical cascade inverter

Veenstra and Rufer investigated *active* charging and balancing strategies for this topology based on the control of common modes of harmonics. The two main innovations in are the use of a three-phase inverter with a common dc-link as high-voltage cell, and the use of the low-voltage cell only as filtering devices, such that they do not require any additional supply. This paper unifies and completes these works by establishing a theory for systematically designing hybrid cascaded multilevel inverters with simplified dc power supply and low losses. It derives a set of design rules that defines six classes of inverters for which an active balance and an efficient modulation can be applied. Single-phase and three-phase topologies exhibit different properties. Inverters with staircase (low frequency) modulation and inverters with PWM (high frequency) are designed in different ways.

II. HYBRID CASCADED MULTILEVEL INVERTER MODEL:

A. Investigated Hybrid Cascaded Multilevel Inverter Topologies:

This paper investigates the design and control of single- and three-phase hybrid cascaded multilevel inverter topologies for which at least two rows have different voltage ratings and switch technologies and for which only the row with the highest voltage is supplied. Examples of such topologies are represented in Figs. 1 and 2. For the three-phase topologies, we only consider structures that combine a supplied three-phase cell with unsupplied single-phase cells as for the topologies represented.

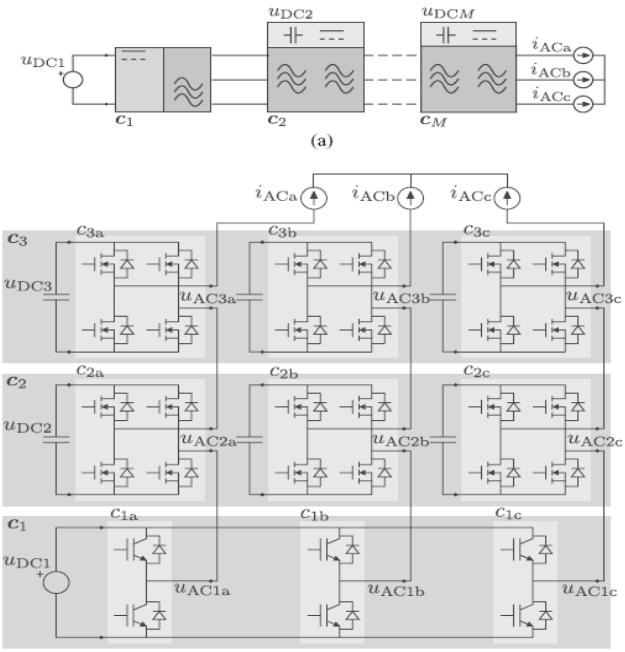


Fig.2. Investigated three-phase inverter topologies combine one three-phase cell with single-phase cells and thus feature a single dc supply. (a) General three-phase topology. (b) Hybrid inverter with two-level three-phase inverter and H-bridges.

The regulation of the voltages of all unsupplied capacitor sin these topologies are complex for two main reasons: First, the energy is stored in capacitors that are distributed both over the phases of the inverter and over the cells within a phase. Second, due to the asymmetry of the dc-voltages, the cells of different voltage ratings need to be coordinated to generate the desired output voltage. For the analysis, the converter is first split between its supplied sub inverter, which is referred to as the high-voltage cell and its unsupplied sub inverter, which is referred to as the low-voltage cell. The main difficulty is the energy balance of the low-voltage cell.

B. Necessary Conditions for Energy Balance:

There are two necessary conditions for regulating the dc voltages of all unsupplied capacitors to their reference value, while tracking the reference voltage and current trajectories.1) The *total* low-voltage cell energy can be regulated only if the low-voltage cell does not provide any active power on average. The high-voltage cell must, therefore, provide the *total* power on average, while the low-voltage cell can *only* provide *reactive, harmonic, and transient powers*. 2) The dc-voltages can be regulated only if the distribution of energy within the low-voltage cell over its phases and rows can be modified, while preserving the inverter target output voltage.

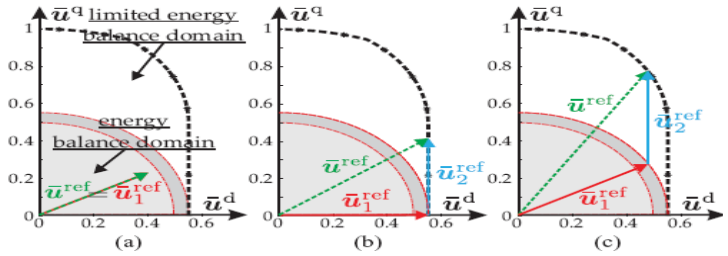


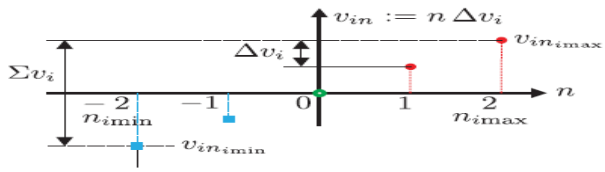
Fig.3.voltage breakdown on average in the dq plane oriented on load current .mode of operation depends on reference magnitude.

These conditions limit the operating range of the converter, and require special design and control procedures that will be developed in Sections III–VI.

C. Operating Modes:

The first necessary condition for balancing the *total* low voltage cell energy requires the high- and low-voltage cells to operate in one of the modes below. 1) For space-vector references smaller than the high-voltage cell maximum magnitude, the high-voltage cell is able to provide the full-voltage on average; the low-voltage cell only needs to provide harmonic filtering that allows it to precisely generate the reference [see Fig. 3(a)]. 2) For space-vector references exceeding the high-voltage cell maximum magnitude, the maximum power factor can be reached by keeping the high-voltage cell contribution parallel to the current, while the low-voltage cell provides a voltage contribution orthogonal to the space-vector current on average, in order to increase the inverter achievable voltage magnitude [see Fig. 3(b)]. 3) The maximum magnitude can be reached by contributing to the orthogonal component of the voltage with both high voltage and low-voltage cells: the achievable power factor is lowest in this mode [see Fig. 3(c)].

The analysis of these operating modes leads to two definitions that will be useful through our developments.*1) Energy balance domain:* This is the set of voltage vectors, represented in light gray in Fig. 3, that can be reached by Achievable power factor and magnitude. In this domain, the ability to exchange power between phases is very limited. The capacitors therefore, need to be sufficiently large to ensure that the voltage ripple remains small while storing the energy required for providing reactive and harmonic power over each cycle. It should be noted that since the generation of reactive currents does not need any active power (on average), the capability of the inverter will always be higher in the *q*-axis as suggest.



4. Key parameters defining the properties of a multilevel cell.

III. DESIGN CONDITIONS FOR ENERGY BALANCE

To balance the low-voltage cell total energy, it is sufficient to operate the converter in one of the three modes described previously in Section II-C. To achieve this, while ensuring that the target space vector is generated at the output of the converter, it is necessary to follow the design rules that will be derived in this section. The keys underlying total and internal balance, while guaranteeing the tracking of the reference level trajectory, independently of the current trajectory, are the design and exploitation of redundant space vectors to adjust the cell power flows. To simplify the explanations, we will consider two series-connected cells, without loss of generality, since we can repeat the reasoning by associating two series-connected cells in a larger cell that would become the new low-voltage cell in the reasoning. In addition, we will exploit the latter property to derive the results presented in Section VIII. We will first derive the design rules for single-phase inverters and then for three-phase inverters.

A. Single-Phase Energy Balance Design Condition:

$$u_{\mathrm{AC}j} = \underbrace{\sum_{i=1}^{M} u_{\mathrm{DC}i}\, s_{ij}}_{\text{level realization } v_o} + \underbrace{\sum_{i=1}^{M} \epsilon_{\mathrm{DC}ij}\, s_{ij}}_{\text{error } \epsilon}. \qquad (1)$$

Each cell *cij* is characterized by its number of levels *Ni* and its nominal voltage step between two adjacent levels Δ*vi*. For the considered inverters, we have Δ*vi* = *u*DC*i*. The level *n* of the cell *cij* is defined as *vin* = *n*Δ*vi* , where *n* is an integer in the interval [*ni*min, *ni*max]. The variables are indexed by the cell row identifier *i*, which is in the range $i \in \{1, \ldots, M\}$, where *M* is the number of series connected cells. The variables are also indexed by the phase identifier *j*, where $j \in \{a, b, c\}$. Since the nominal levels *vin* do not depend on the phase index *j*, they are only indexed by the row number *i*. The cell output voltage *u*AC*ij* is controlled by the signal denoted *sij*, yielding *u*AC*ij* = *vin* when *sij* = *n* (see Fig. 4). The types and number of series-connected cells define the topology, while the selected nominal dc-voltages determine the *configuration* of a given topology.

Considering that an elementary cell is a balanced sub inverter, the topology and the configuration are defined by the number of levels and voltage steps of all cells, which is written compactly as *{(N*1 *,*Δ*v*1 *), . . . , (NM ,*Δ*vM)}*. The topology of the cells can be omitted in the present analysis as they do not affect the output voltages nor the energy balance mechanisms. The levels of one phase are obtained by summing the contributions of the *M* series-connected cells.

We call a realization of the target level *vo* a combination of switch control signals that lead to this level in the absence of voltage error. Distinct realizations of the same level *vo* are called redundant levels. From (1), it is clear that redundant levels *rigorously exist* only in the absence of imbalance and conduction losses. We will investigate in details how to deal with voltage errors later in Section VI. In the first part of the investigation, we will neglect the voltage error. By considering two distinct levels, *v*1*k* and *v*1*m*, of the high-voltage cell and two distinct levels, *v*2*l* and *v*2*n* , of the low-voltage cell, the redundant realizations of the target level *vo* of the inverter formed by these two cells satisfy the relation

$$\underbrace{v_{1k} + v_{2l}}_{\text{first realization of } v_o} = \underbrace{v_{1m} + v_{2n}}_{\text{second realization of } v_o} = v_o. \qquad (2a)$$

Consistently with the definitions of the levels previously in Fig. 4, the indices *k* and *m* are different integers in the same interval [*n*1min, *n*1max], while *l* and *n* are different integers in the same interval [*n*2min, *n*2max]. By modulating these different realizations of the target level *vo* with the duty cycle *λ*, the low voltage cell average voltage contribution to *vo* , denoted $\bar{u}$AC2 can take any value between *v*2*l* and *v*2*n* Since the current is the same for all cells of the same phase, the average power can take any value between *v*2*l i*AC*j* and *v*2*n i*AC*j* by adjusting *λ*, given the output voltage and current. We consider three possible cases that depend on the signs of *v*2*l* and *v*2*n* . 1) If *v*2*l* and *v*2*n* are of opposite sign, then the low-voltage cell power can take positive or negative value by manipulating *λ*. This implies the possibility of reversing the power in order to correct the energy stored in the considered low-voltage cell independently of the current trajectory.

The magnitude of the possible correction depends on the magnitude of the current. 2) If one of the two levels, e.g., *v*2*l* , is equal to zero, then it follows that the power is constrained to be between *+1* zero and *v*2*n i*AC*j* As a consequence, the errors can be corrected only in the direction opposite to *v*2*n i*AC*j*. The capacitor energy can, however, be kept constant. 3) If *v*2*l* and *v*2*n* have the same polarity, it is not possible to reverse or cancel the power in the low-voltage cell. Any current will eventually lead to an imbalance. It is not possible to permanently operate in these conditions. It is possible to employ the associated levels only if the current trajectory allows one to cancel the error. According to the three cases identified previously, the hybrid multilevel inverter should be designed such that: 1) each level must have at least two realizations fulfilling cases 1 or 2;2) the levels that only have one realization should not contribute to the output voltage. Following these rules, the energy stored in the low-voltage cell can be regulated. This can be achieved for all levels between any pair of adjacent levels of the high-voltage cell *v*1*k* and *v*1*k by* fulfilling the condition.

$$\Delta v_1 \leq \frac{N_2 + 1}{2} \Delta v_2 .$$

This condition can be understood by examining how the cells contribute to the levels on the state-space representations of Fig. 5(a) and (b). Fulfilling condition (3) means that the inverter can be balanced for arbitrary currents, for all levels in the interval [*v*1*n*1m in , *v*1*n*1m a x]. This interval forms the energy balance domain of the inverter that was defined in Section II-C1. The levels that are outside this interval are either not redundant or belong to case 3 described previously: the inverter can be balanced outside this interval only for specific voltage and current trajectories.

B. Three-Phase Energy Balance Design Condition:

For three-phase topologies, we consider together the cells of the same row of index *i* to form three-phase cells. The cell formed by grouping *ci*a , *ci*b and *ci*c is denoted ***ci*** The space vectors generated by the three-phase cell ***ci*** are obtained by summing the space-vector contributions over the rows of the converter

$$u_{\mathrm{AC}i} = u_{\mathrm{DC}i} s_i + \epsilon_i \tag{4a}$$

with the vector-valued switching signal

$$s_i = T^{\alpha\beta}_{\mathrm{abc}} \begin{bmatrix} s_{i\mathrm{a}} & s_{i\mathrm{b}} & s_{i\mathrm{c}} \end{bmatrix}^T$$

and the deviation from the nominal target ***vo***

$$\epsilon_i = T^{\alpha\beta}_{\mathrm{abc}} \begin{bmatrix} s_{i\mathrm{a}}\epsilon_{\mathrm{DCa}} & s_{i\mathrm{b}}\epsilon_{\mathrm{DCb}} & s_{i\mathrm{c}}\epsilon_{\mathrm{DCc}} \end{bmatrix}^T$$

where ***Tαβ***
abc is the coordinate transformation matrix. The power transmitted by the cell ***ci*** is expressed as

$$p_{\mathrm{AC}i} = u^T_{\mathrm{AC}i}\, i_{\mathrm{AC}}.$$

It is important to observe that even if the single-phase cells *cij* have no redundant level, the three-phase cell ***ci*** has redundant space vectors due to the absence of neutral connection, which is reflected by the suppression of the common mode through the

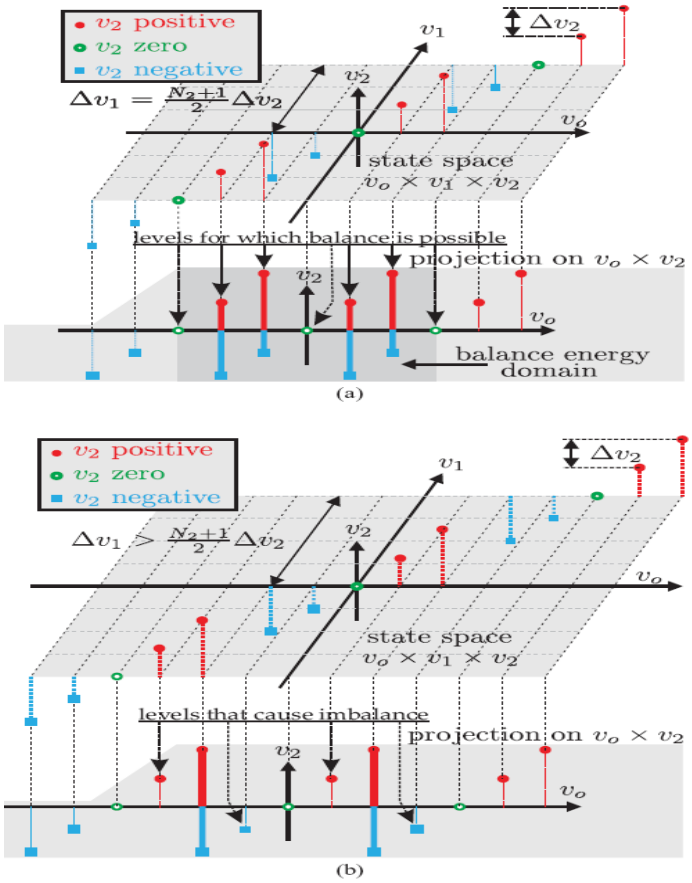


Fig. 5. State-space representation of levels illustrating design condition (3) for the combination of two cells.

Vertical: low-voltage cell levels, third axis in perspective high-voltage cell levels, horizontal axis generated levels. (a) Configuration *{*(3,3), (5,1)*}* fulfills condition (3). (b) Configuration *{*(3,4), (5,1)*}* does not fulfill condition (3) coordinate transformation ***T*** *αβ* abc Since changing the common mode voltage of the three-phase cell ***ci*** generates redundant space vectors, (4d) means that the common-mode voltage does not affect the total power of the considered cell. This is the main reason why the single- and three-phase design rules are different. The common mode affects, however, the balance between the phases of this cell. These properties will

be exploited to decouple the regulation of the total energy stored in the capacitors of the three-phase cell ***ci*** and the internal balance of its individual cells *ci*a , *ci*b , and *ci*c as will be discussed in Section V. The total output space vector is obtained by the summation of the space vectors over all cells.

$$\boldsymbol{u}_{\mathrm{AC}} = \underbrace{\sum_{i=1}^{M} \boldsymbol{u}_{\mathrm{AC}i}}_{\text{target space vector } \boldsymbol{v}_o} + \underbrace{\sum_{i=1}^{M} \boldsymbol{\epsilon}_i}_{\text{error } \boldsymbol{\epsilon}} .$$

(5)

Similarly to the single-phase case, redundant realizations of the space vector ***v****o* rigorously exist only in the absence of imbalance and losses. The redundant realizations of the target space vector ***v****o* are defined as

$$\underbrace{\boldsymbol{v}_o}_{\text{target}} = \underbrace{\boldsymbol{v}_{1k_r} + \boldsymbol{v}_{2l_r} \quad \forall r}_{\text{redundant space vector of index } r} .$$

(6a)

The different realizations are modulated in order to balance the energy of the low-voltage cell. *kr* and *lr* are the indices of the low- and high-voltage cell space vectors that lead to the realization identified by the index *r*. This realization is applied with the duty cycle λr . The average contributions of the low voltage and high-voltage cells to the output voltage are

$$\bar{u}_{\mathrm{AC1}} = \sum_{r=1}^{3} \lambda_r v_{1k_r} \quad \bar{u}_{\mathrm{AC2}} = \sum_{r=1}^{3} \lambda_r v_{2l_r} \quad \sum_{r=1}^{3} \lambda_r = 1$$

(6b)

$$\sum_{r=1}^{3} \lambda_r \boldsymbol{v}_{2l_r} \boldsymbol{i}_{\mathrm{AC}} = 0 \qquad (7a)$$

for increasing it

$$\sum_{r=1}^{3} \lambda_r \boldsymbol{v}_{2l_r} \boldsymbol{i}_{\mathrm{AC}} < 0 \qquad (7b)$$

for decreasing it

$$\sum_{r=1}^{3} \lambda_r \boldsymbol{v}_{2l_r} \boldsymbol{i}_{\mathrm{AC}} > 0. \qquad (7c)$$

Respectively. The duty cycles are computed to regulate the low voltage cell dc-voltage through the control of the low-voltage cell average contribution ***u***AC2 to the target space vector ***v****o*. For maintaining the low-voltage cell dc-voltage constant, we must impose

Compared to the single-phase case, the first difference is that it is necessary to modulate at least three space vectors to manipulate the contribution of the low-voltage cell as desired. The second difference is that the contribution of the low-voltage cell needs to be oriented with respect to the space-vector current [Fig. 2(b)]

$$\boldsymbol{i}_{\mathrm{AC}} = T_{abc}^{\alpha\beta} \begin{bmatrix} i_{\mathrm{ACa}} & i_{\mathrm{ACb}} & i_{\mathrm{ACc}} \end{bmatrix}^T .$$

To regulate the low-voltage cell capacitor voltages, the relation that is fulfilled in (7) must be controllable independently of the orientation of the current. The control has to be done by selecting the appropriate modulated space vectors ***v***2*lr* and the associated duty cycles λr . This controllability is obtained if the direction of the low-voltage cell contribution with respect to the current direction can be controlled independently of the hybrid inverter total output voltage.

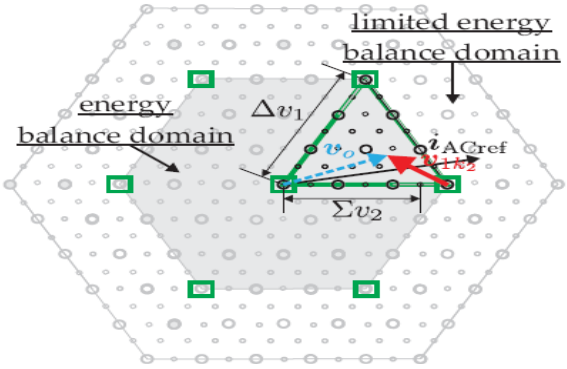


Fig.6. Investigated three-phase topologies generate a number of space vectors growing with the number of series connected cells:

The two-level three-phase inverter generates seven space vectors (rectangles); adding one cell consisting of three generates 54 more space vectors (large circles); adding another cells.

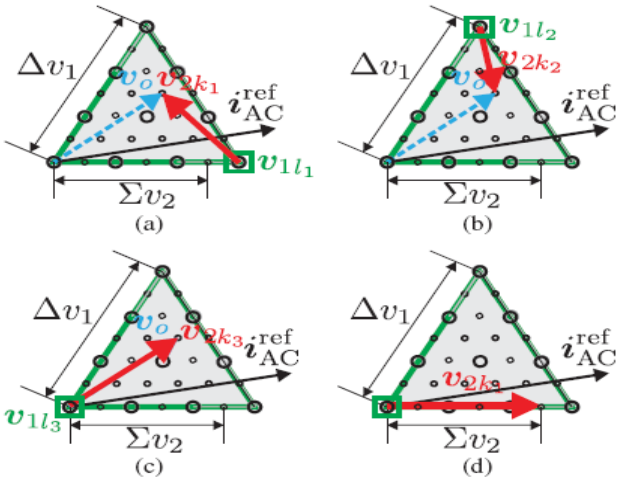


Fig.7. Modulation of the realization of the target space vector ***v o*** allows to orient arbitrarily the contribution of the low-voltage cell with respect to the current vector. (a) ***v o*** first realization. (b) ***v o*** second realization. (c) ***v o*** third realization. (d) Worst case fulfilling condition (8).

The design condition to obtain balance of the low-voltage cell is derived by investigating the controllability of the direction of the low-voltage cell contribution. In Fig. 6(a)–(d), the different options for synthesizing a target space vector ***v o*** are investigated. If the space vectors strictly inside this triangle can be generated in three different ways, each activating one of the three adjacent space vectors of the high-voltage cell, as illustrated in Fig. 7(a)–(c), then it is clear that the modulated low voltage cell contribution built using (6) can take any direction. The space vectors that are on the corners of the area do not need to be redundant since the contribution of the low-voltage cell to these is zero for these. The other space vectors on the side of the area need to have two realizations: this is where the contribution of the low-voltage cell needs to be the largest, which yields the worst case illustrated in Fig. 7(d). The associated design condition derived based on the worst case constrains the high-voltage cell step and the low-voltage cell magnitude as follows:

$$\Delta v_1 \leq N_2 \Delta v_2. \qquad (8)$$

Condition (8) repeatedly to form inverters with more than two cells yields the condition

$$\Delta v_i \leq \sum_i N_{i+1} \Delta v_{i+1}. \qquad (9)$$

Applying conditions (8) or (9) to design the inverter guarantees that the low-voltage cell total energy can be balanced for arbitrary current trajectories, for which the voltage trajectory remains within the energy balance domain. The energy balance domain is the area formed by the convex envelop of the space vectors of

the high-voltage cell represented by the gray area in Fig. 6. To allow internal balance over the phases, the voltage and current trajectories must be cyclic. Outside the energy balance domain power factor restrictions apply.

IV. DESIGN CONDITIONS FOR ENERGY BALANCE AND LOW SWITCHING LOSSES:

In the previous section, design rules that guarantee sufficient redundant realizations for each level and space vectors to regulate the voltages of the low-voltage cells were derived. The modulation of redundant vectors was used to balance the cells. PWM operation of different voltage vectors to smoothly control the output voltage can readily be superimposed using the same balancing concepts, but it may result in excessive switching losses due to the operation of the high-voltage cells at the PWM frequency. Design conditions to operate the high-voltage cells at low switching frequency have already been derived for single- and for three-phase inverters but without considering energy balance. This section derives design rules that allow the low-voltage cell energy balance and the optimal operation of the high-voltage cell at low switching frequency

A. Double Modulation Principle:

The balance principle elaborated in the previous section modulates redundant realizations of the target space vector ***v****o* with the duty cycles λr to control the low-voltage cell stored energy by manipulating the output voltage breakdown over the cells. It is worth stressing the difference between this balance modulation and the synthesis of a reference space-vector voltage $u_{\mathrm{AC}}^{\mathrm{ref}}$ using PWM. The first does not affect the output voltage, while the latter requires the modulation of several space vectors with the duty cycles ***d***. To synthesize a reference space-vector voltage using PWM, while regulating the unsupplied capacitor Voltages $u_{\mathrm{AC}}^{\mathrm{ref}}$ two modulations with two different objectives need to be combined.

The modulation that regulates the dc voltages does not need to be very fast, since it deals with the balance of relatively large capacitors with long time constants, while the synthesis of the target space vector needs to be very fast since it usually deals with fast dynamics. By design, the balancing modulation requires that the high-voltage cell switches when the inverter switches from one realization of a space vector to another. In the ideal case, it would be necessary to switch the high-voltage cell space vector only at low frequency, either for

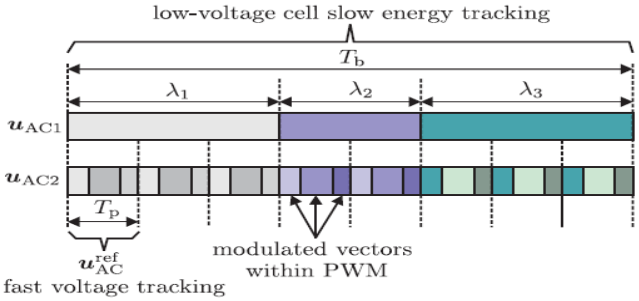


Fig.8. Double modulation principle:

The duty cycles $\lambda 1,2,3$ that allow one to regulate the capacitor voltages and the duty cycles $d1,2,3$ that allow one to synthesize the reference are operating at two different frequencies in order to minimize the hybrid inverter switching losses. the balance or when changing the set of modulated space vectors, but not during the output space-vector

Synthesis that would require operation at the PWM frequency. The corresponding double modulation principle is represented in Fig. 8. We will investigate how to design the inverter to be able to apply this double modulation with two different switching frequencies in Sections IV-B and IV-C.

B. Single-Phase Energy Balance and Low-Switching Loss Design Condition:

To synthesize the reference *u*ref AC, the PWM generator modulates two adjacent levels *vo* and *vo* $+\Delta v2$ with the duty cycle

$$u_{\mathrm{AC}}^{\mathrm{ref}} = v_o + d\,\Delta v_2. \qquad (10)$$

In order to keep the switching losses low, this modulation procedure should be carried out without switching the high-voltage cell. This means that the duty cycle should modulate only the low-voltage cell levels *v2l* and *v2l* +Δ*v*2 . This is possible only if (10) can be rewritten as

$$u_{AC}^{ref} = v_{1k} + v_{2l} + d\,\Delta v_2. \qquad (11)$$

Both *v2l* and *v2l* +Δ*v*2 need to be feasible levels of the low voltage cell. In order to be able to balance the capacitor voltage, another realization of the modulated levels that can be written in the form (11) and that reverses the contribution of the low voltage cell should exist

$$u_{AC}^{ref} = v_{1m} + v_{2n} + d\,\Delta v_2, \quad v_{1m} = v_{1k} + \Delta v_1. \qquad (12)$$

V2n and *v2n* +Δ*v*2 need to be feasible levels of the low voltage cell. In (11) and (12), the fact that the duty cycle *d* is only a factor of the low-voltage cell levels reflects that the high voltage cell is not operated at the PWM switching frequency. The high-voltage cell switches only when modulating between (11) and (12) with the duty cycle λ to balance the low-voltage cell energy. The average contributions of the high-voltage and low-voltage cells are

$$\bar{u}_{AC1} = \lambda v_{1k} + (1-\lambda) v_{1m} \qquad (13a)$$

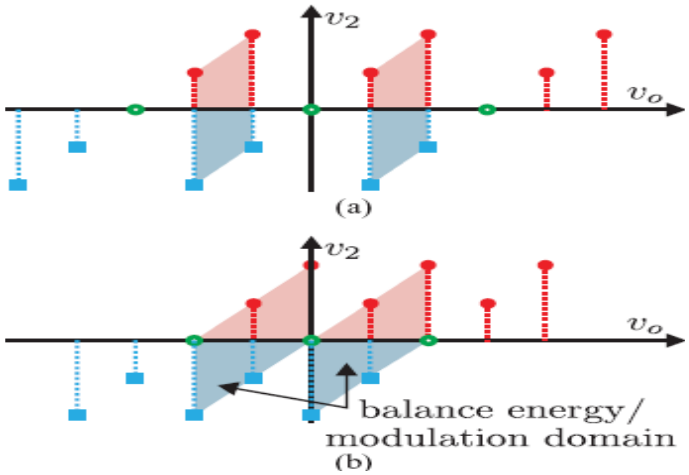


Fig.9. Combination of the level of two cells for three different cases, leading to different balance and optimization possibilities.

(a) Power balancing capability

for $\Delta v_1 = \frac{N_2+1}{2}\Delta v_2$. (b) Power balancing capability for $\Delta v_1 = \frac{N_2-1}{2}\Delta v_2$.

$$\bar{u}_{AC2} = \lambda v_{2l} + (1-\lambda) v_{2n} + d\,\Delta v_2. \qquad (13b)$$

Since it is by construction necessary to switch the high voltage cell levels *v*1*k* and *v*1*m* during balance operation, when switching between (11) and (12) with the duty cycle λ, the associated modulation should be performed at a frequency sufficiently low to obtain reduced switching losses. The achievable frequency depends on the available capacitance. The condition for the existence of at least two different realizations in the form (11) and (12) is written

$$\Delta v_1 \le \frac{N_2 - 1}{2}\Delta v_2. \qquad (14)$$

This condition can be understood by comparing the breakdown of the voltage over the cells on the state-space representation of Fig. 9(a) and (b) for two different inverter configurations. The energy balance and optimized modulation domain is the interval defined by the lowest and highest levels of the high-voltage cell.

C. Three-Phase Energy Balance and Low-Switching Loss Design Condition

The results from previous section are extended to yield less restrictive design conditions valid for three-phase inverters. Similarly to what has been done in Section III-B, the reference must have three distinct realizations generated based on three different space vectors of the high-voltage cell, as illustrated in Fig. 10(a)–(c). The design condition that allows this to be obtained is deduced from the worst case illustrated in Fig. 10(d)

$$\Delta v_1 \leq (N_2 - 1)\Delta v_2. \qquad (15)$$

Condition (15) can be applied repeatedly

$$\Delta v_{i+1} \leq \sum_i (N_i - 1)\Delta v_i. \qquad (16)$$

In the energy balance and modulation domain formed by the largest voltage vectors of the high-voltage cell, it is possible to apply the double modulation represented in Fig. 8

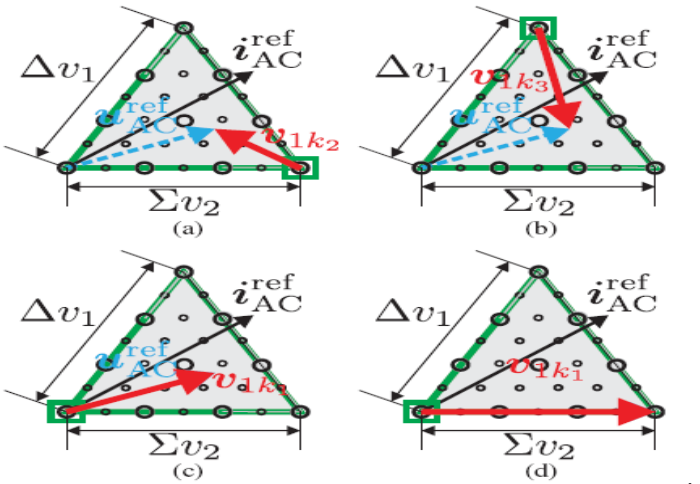


Fig.10. Illustration of the Design rule for voltage balance and low switching losses of multiphase hybrid multilevel inverters. (a) ***u***ref AC first realization. (b) ***u***ref AC second realization. (c) ***u***ref AC third realization. (d) Worst case fulfilling condition (15).

V. THREE-PHASE LOW-VOLTAGE CELL INTERNAL BALANCE OVER PHASES:

In Sections III-B and IV-C conditions for guaranteeing the regulation of the *total energy* of the three-phase low-voltage cell were derived. The capacitor could be arbitrarily small and its size would only be limited by the desired high-voltage cell switching frequency. The balance of the total energy, however, does not guarantee internal balance over the phases. The total stored energy cannot be arbitrarily small because there is an unavoidable ripple linked to the current and voltage trajectories. Internal balance over the phases can be done separately from the total energy balance by manipulating the components of the voltage orthogonal to the current vector, i.e., the components of the voltage vector that yield.

$$\begin{bmatrix} u^{\perp}_{ACia} & u^{\perp}_{ACib} & u^{\perp}_{ACic} \end{bmatrix} \begin{bmatrix} i_{ACa} & i_{ACb} & i_{ACc} \end{bmatrix}^T = 0. \quad (17)$$

The components of the voltage vector described by (17) can be separated in the common-mode voltage component ***u***AC*i*0 and in the voltage vector orthogonal to the current in the $\alpha\beta$ plane. The latter satisfies the relation u_{ACi0}

$$u_{\mathrm{ACi}}^{\perp\,T} i_{\mathrm{AC}} = \left[u_{\mathrm{ACi}\alpha}^{\perp} \quad u_{\mathrm{ACi}\beta}^{\perp}\right]\left[i_{\mathrm{AC}\alpha} \quad i_{\mathrm{AC}\beta}\right]^{T} = 0. \quad (18)$$

A. Compensation through Common-Mode V oltage:

The main attraction of manipulating the common-mode voltage component for balancing the energy over the phases is that this can be performed separately, without affecting the output voltage and without affecting the contribution of the high-voltage cell. The relation governing the power variations through the common-mode voltage is

$$\Delta p_{\mathrm{a}} = u_{\mathrm{ACi0}}\, i_{\mathrm{ACa}} \quad (19a)$$

$$\Delta p_{\mathrm{b}} = u_{\mathrm{ACi0}}\, i_{\mathrm{ACb}} \quad (19b)$$

$$\Delta p_{\mathrm{c}} = u_{\mathrm{ACi0}}(-i_{\mathrm{ACa}} - i_{\mathrm{ACb}}) \quad (19c)$$

the common-mode voltage is constrained through the relations

$$-\frac{N_i - 1}{2} u_{\mathrm{DC}ij} \le u_{\mathrm{AC}ij} + u_{\mathrm{ACi0}} \le \frac{N_i - 1}{2} u_{\mathrm{DC}ij}$$

$$\forall j \in \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}. \quad (19d)$$

The constraints (19d) mean that the smaller the magnitude of the voltage of the low-voltage cell, the larger the achievable magnitude for the common-mode voltage component *u*AC*i*0: there is no imbalance correction capability when the low-voltage cell output is saturated. Since the common-mode voltage is coupled to the three phases in the same way, it is not possible to compensate simultaneously the three phases. This is not a strong restriction since the load currents are also coupled in the same way.

The losses may lead to uncoupled imbalances due to parameter mismatch. Switching losses, however, tend to mitigate imbalances since they increase with the dc voltage. When the low-voltage cell is controlled through PWM, *u*AC*i*0 can be manipulated continuously. Since one variable is used to correct two imbalances and since it is constrained, the best is to employ an optimization procedure to select *u*AC*i*0 optimally: this can be solved explicitly and this is an approach that has been adopted for he experimental results presented in Section

VIII. THE IMPLEMENTED APPROACH IS BASED ON SOLVING EXPLICITLY THE FOLLOWING OPTIMIZATION PROBLEM:

$$\min_{u_{\mathrm{ACi0}}(t)} \sum_{j \in \mathrm{a,b,c}} e_{ij}(t + T_{\mathrm{h}})^2 \quad \text{subject to (19d).} \quad (19e)$$

The energy error *eij* of cell *cij* at time *t* is computed based on voltage measurements and dc-reference voltage. The dynamics of the errors employed to compute the solution to (19e) are modeled as follows:

$$e_{ij}(t + T_{\mathrm{h}}) = e_{ij}(t) + \left(u_{ij}^{\mathrm{ref}}(t) + u_{\mathrm{ACi0}}(t)\right) i_{\mathrm{AC}j}(t) T_{\mathrm{h}}. \quad (19f)$$

The currents and voltages are assumed to be constant over the horizon *T*h . Due to this assumption, the horizon length should not be longer than a few sampling periods.

B. Compensation in the αβ Plane.

Since the output voltage must not be affected by the regulation of the dc voltages, the manipulation of the component orthogonal to the current in the *αβ* plane needs to be done in a complementary way on the high- and low-voltage cells. Operating in a complementary way with the high-voltage cell means that this can be done

only slowly in an average sense. Moreover, compensation in the *αβ* plane decreases the available magnitude of the high-voltage cell. It cannot be done for magnitudes close to the maximum achievable magnitude in the energy balance domain. For these reasons, balance through the common mode is preferred and is the only applied principle for correcting phase imbalance in Section VIII, but additional compensation of imbalance with compensation in the *αβ* plane can be envisaged to improve the overall balance, for instance by reducing the ripple for known trajectories.

VI. ROBUST DESIGN AND CONTROL CONCEPTS UNDER POWER LOSSES AND DC-VOLTAGE IMBALANCES

In Sections III and IV, the dc-voltage fluctuations and conversion losses were neglected in the derivations of the dc-voltage design conditions. Their impacts are a deviation of all feasible levels or space vectors from their nominal values and the separation of the redundant space vectors that become all distinct, as described by (1) and (5). This section extends the design conditions (14) and (15) to be valid under voltage imbalances and conversion losses. *A. Large Imbalance Compensation in Single-Phase Systems* By applying the energy control modulation, two different realizations of the same nominal PWM pattern are modulated

$$\tilde{u}^1_{\mathrm{AC}} = \underbrace{v_{1k} + v_{2l} + d\,\Delta v_2}_{u^{\mathrm{ref}}_{\mathrm{AC}}\ \text{nominal reference}} + \underbrace{\sum_{i=1}^{N} s_{ij1}\epsilon_{DCij} + d\epsilon_{DC1j}}_{\epsilon_1 := \bar{u}^1_{\mathrm{AC}}\ \text{voltage mismatch}}$$

$$\tilde{u}^2_{\mathrm{AC}} = \underbrace{v_{1m} + v_{2n} + d\,\Delta v_2}_{u^{\mathrm{ref}}_{\mathrm{AC}}\ \text{nominal reference}} + \underbrace{\sum_{i=1}^{N} s_{ij2}\epsilon_{DCij} + d\epsilon_{DC1j}}_{\epsilon_2 := \bar{u}^2_{\mathrm{AC}}\ \text{voltage mismatch}}.$$

The nominal waveforms associated with $\tilde{u}^1_{\mathrm{AC}}$ and $\tilde{u}^2_{\mathrm{AC}}$ AC are identical; however, due to the voltage mismatches, the synthesize voltages are different. Modulating two different realizations, $\tilde{u}^1_{\mathrm{AC}}$ and $\tilde{u}^2_{\mathrm{AC}}$, AC, of the reference, *u*ref AC, allows the low voltage cell energy to be balanced. The modulation of two different voltage mismatches causes voltage steps at the balance modulation frequency that result in a distortion of the output voltage. The remedy to slow dc-voltage variations usually consists in adjusting the duty cycles in order to correct these fluctuations; however, it can be applied to the multilevel case only if some design conditions are fulfilled. Indeed, the voltage mismatch could be achieved by applying corrected duty cycles solving.

$$\tilde{v}_{1k} + \tilde{v}_{2l} + d^1\,\Delta\tilde{v}_2 = u^{\mathrm{ref}}_{\mathrm{AC}} \qquad (21a)$$

$$\tilde{v}_{1k} + \Delta\tilde{v}_1 + \tilde{v}_{2l} + d^2\,\Delta\tilde{v}_2 = u^{\mathrm{ref}}_{\mathrm{AC}} \qquad (21b)$$

Where ˜*vij* and Δ˜*vi* are the values of the voltage levels, respectively, steps of the converter cells that can readily be obtained from the measured dc voltages. Solving (21), two distinct duty cycles *d*1 and *d*2 are obtained

$$d^1 = \frac{u_{\mathrm{AC}} - \tilde{v}_{1k}(t) - \tilde{v}_{2l}(t)}{\Delta\tilde{v}_2} \qquad (22a)$$

$$d^2 = \frac{u_{\mathrm{AC}} - \tilde{v}_{1k}(t) - \Delta\tilde{v}_1 - \tilde{v}_2(t)}{\Delta\tilde{v}_2}. \qquad (22b)$$

It is possible to apply this correction only if the resulting duty cycles are both feasible, which means they both fulfill $0 \le di \le 1$, which is possible only if the following conditions are satisfied:

$$\tilde{v}_{1k} + \tilde{v}_{2l} \leq u_{AC}^{ref} \leq \tilde{v}_{1k} + \tilde{v}_{2l} + \Delta\tilde{v}_2 \qquad (23a)$$

$$\Delta v_2 \geq \left(\frac{2}{N_2 - 1} + \frac{\bar{\epsilon}_{DC1}}{\Delta v_1} + \frac{N_2 - 1}{2} \frac{\bar{\epsilon}_{DC2}}{\Delta v_1} \right) \Delta v_1 . \qquad (24)$$

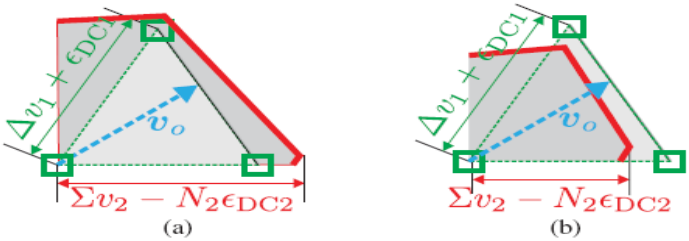


Fig 11. Illustration of voltage-balance condition with voltage error. (a) Condition (25) is fulfilled: all references can be reached. (b) Condition (25) is not fulfilled: references outside the thick polygon cannot be reached.

$$\tilde{v}_{1m} + \tilde{v}_{2n} \leq u_{AC}^{ref} \leq \tilde{v}_{1m} + \tilde{v}_{2n} + \Delta\tilde{v}_2 . \qquad (23b)$$

This can be achieved for all feasible references only if the condition (14) is satisfied for all possible voltage fluctuations, which yields in the worst case.

B. Three-Phase Case :

The reasoning for the three-phase case is very similar. The inverter reachable domain is no longer a fully symmetrical hexagon. The triangles formed by adjacent space vectors are no longer equilateral as illustrated graphically in Fig. 11. To guarantee the ability to balance voltages for all references, it is necessary to increase the low-voltage cell nominal voltage such that its reachable domain covers the triangle formed by three adjacent space vectors of the high-voltage cell as illustrated graphically in Fig. 11(a). The design conditions is found by computing the worst case error as previously, which is written compactly as

$$\Delta v_2 \geq \frac{\Delta v_1}{N_2 - 1} + \max_{i,j} \left| \epsilon_{2i} - \epsilon_{2j} \right| . \qquad (25)$$

The interpretation of the robust design conditions (24) and (25) is that by (slightly) increasing the nominal voltage of the low-voltage cell according to the maximum fluctuations of the high- and low-voltage cell dc voltages, it is possible to apply the balance concepts derived in the previous section despite large imbalances and losses.

VII. SUMMARY AND PERFORMANCE EVALUATION

A. Hybrid Cascaded Multilevel Inverter Design:

1) Design of the Inverter Configuration: The design rules that have been derived in the previous sections are summarized in Table I. The rules of Section IV are omitted since they are equivalent to the robust rules derived in Section VI when _ = 0. As there are infinitely many inverter configurations fulfilling conditions (26) of Table I, some additional design constraints are imposed: a) the number of different cells is limited to 2 for modularity.

TABLE I
OVERVIEW OF DESIGN RULES

	Energy balance	**Robust energy balance /optimized modulation**
1-phase	$\Delta v_1 \leq \frac{N_2+1}{2}\Delta v_2$ (26a) section III-A	$\Delta v_2 \geq \frac{2\Delta v_1}{N_2-1}+\epsilon$ (26b) sections IV-B and VI-A
3-phase	$\Delta v_1 \leq N_2 \Delta v_2$ (26c) section III-B	$\Delta v_2 \geq \frac{\Delta v_1}{N_2-1}+\epsilon$ (26d) sections IV-C and VI-B

TABLE II
EXAMPLES OF INVERTER CONFIGURATIONS DESIGNED WITH (26)

	M	N	N_1		Δv_1	N_2	Δv_2	N_3	Δv_3	N_4	Δv_4
Single-phase inverter configurations designed with (26a)											
(a)	2	7	3		2	3	1				
(b)	3	11	3		3	3	1	3	1		
(c)	4	15	3		4	3	1	3	1	3	1
Single-phase PWM inverter configurations designed with (26b)											
(a)	2	5	3		1	3	1				
(b)	3	7	3		2	3	1+ϵ	3	1+ϵ		
(c)	4	11	3		3	3	1+ϵ	3	1+ϵ	3	1+ϵ
Three-phase inverter configurations designed with (26c)											
(a)	2	6	2	(3p. inv.)	2	3	1				
(b)	3	10	2		5	3	1	3	1		
(c)	4	14	2		7	3	1	3	1	3	1
(d)	2	9	3	(3p. NPC)	3	3	1				
(e)	3	15	3		5	3	1	3	1		
(f)	4	21	3		7	3	1	3	1	3	1
Three-phase PWM inverter configurations designed with (26d)											
(a)	2	5	2	(3p. inv.)	2	3	1+ϵ				
(b)	3	9	2		4	3	1+ϵ	3	1+ϵ		
(c)	4	13	2		6	3	1+ϵ	3	1+ϵ	3	1+ϵ
(d)	2	7	3	(3p. NPC)	2	3	1+ϵ				
(e)	3	13	3		4	3	1+ϵ	3	1+ϵ		
(f)	4	19	3		6	3	1+ϵ	3	1+ϵ	3	1+ϵ

only the most asymmetrical configurations are considered for each topology for maximizing the achievable power factor; c) in the three-phase inverters, the high-voltage cell is either a two-level or a three-level NPC to avoid its internal balancing issues; d) all other cells are H-bridge inverters; e) at most four series connected cells are considered. Applying the design rules of Table I with these design constraints, we obtain the configurations listed in Table II. Comparing the three-phase inverter and three-phase PWM inverter configurations, it appears that the difference in terms of number of levels becomes marginal as the number of cells Switching losses can be saved at nearly no cost in resolution by applying (16) rather than (9). It is worth noting that it is possible to derive more asymmetrical configurations than these proposed in Table II; however, limiting the types of cells to two increases modularity while retaining the key properties of hybrid multilevel inverters. It, moreover, makes the realization of the balance software easier.

The control of the three-phase PWM inverter configuration (b) has been investigated in. Sliding-mode control was employed to balance the energy. The control of the three-phase inverter configuration (d) has been investigated in details in. Harmonics of the common-mode voltage reference were manipulated to balance all the voltages. The main practical results in this study are new inverter configurations that open new design possibilities as many more switch voltage ratings in C using a DSP board with a DSP from Analog Device (Sharc ADSP 21062 40 MHz). The multilevel PWM is implemented using an on-board FPGA from Xilinx (Spartan XCS-40). The control algorithms were tested on an induction motor drive. The drive stator voltage reference was obtained applying the field-oriented model predictive torque controller presented in. The three-phase PWM inverter configurations (a) and (b) of Table II are tested under various transient and steady-state conditions. The next two sections illustrate the balancing capabilities during transients as well as the quality of waveforms during the steady-state operation.

B. Five-Level Hybrid Cascaded Multilevel:

Inverter Drive Results:

In this section, the performance of the three-phase PWM inverter configurations (a) of Table II is evaluated. This topology is as the topology in Fig. 2(b) when removing the third cell $\boldsymbol{c}3$. In this configuration,

the setup is limited by the rating of the MOSFETs: applying (26d) with *u*DC2 =50 V and _ =5 V, the nominal high-voltage cell dc voltage is obtained *u*DC1 ≈ 90 V.

1) Voltage Regulation during Pre charge:

Fig. 14 demonstrates the good regulation of the dc voltages. Fig. 14(a) shows the pre charge of the three capacitors. During the pre charge, condition (8) is not fulfilled and it is necessary to switch the high-voltage cell at the PWM frequency. The pre charge current and the PWM frequency are, therefore, selected smaller than their rated values (1 kHz, 2 A).

2) Voltage Regulation during Normal Operation:

Upon completion of the pre charge, in Fig. 14(b), the PWM frequency is set to 2 kHz and the high-voltage cell is switched at most at three times the fundamental frequency. In Fig. 14(b)-(d), we can see that the high-voltage cell is operated at three times the m fundamental frequency at low and medium speed and at the fundamental frequency at high speed. The maximum switching frequency is, therefore, around 60 Hz: this maximum frequency appears before the drive switches from four to two pulses per period on the line-to-line voltage and when the drive operates be selected and systematic and robust design rules and effective control strategies for these configurations. 3) Selection of the Semiconductor Devices

One of the main differences with cascade symmetrical multilevel inverter topology is that the switching frequency depends on the cell voltage rating, i.e., on its row index *i*. For the low-voltage cells, the design is, however, very similar to other PWM voltage-source inverters. The best tradeoff between switching losses, conduction losses, and possibly other criteria such as cost has to be found. For the high-voltage cells, the fact that they inherently switch slowly mostly affects the selection of the switch type: as their switching losses only marginally affect the overall losses, switching devices with low ratio between conduction losses and switching losses are preferred. Since the thermal energy to be transferred out of the high-voltage cells through the cooling system will be smaller than for other topologies, this allows a slight reduction of the cooling and/or current rating of the cell.

B. Feasible Operating Range:

It has been shown in Section II-C that the energy balance restrains the inverter operating modes and range. One of the most important arguments for the selection of the configuration is the achievable operating range in terms of power factor. One way of evaluating this is to compute the ratio between the radius of the energy balance domain and the radius of the total inverter voltage

The ratio on the left-hand side of the inequality depends on the selected configuration. Its upper limit on the right-hand side of the inequality only depends on the number of levels of the high-voltage cell. It is attained when the upper limit of condition (26d) is attained. The main interpretation of (26) is that the voltages for which the inverter energy can be balanced without restriction on the power factor increase with and only depends on the number of levels of the high-voltage cell. Fig. 12 shows the theoretical achievable operating range as a function of the number of levels of the (supplied) high-voltage cell for the most asymmetrical configurations (configurations with *N*1 = 2, 3 are shown in Table II). Fig. 13 shows the actual operating range achievable by the three-phase PWM inverter configurations (a)- (c) from Table II. Given their limited achievable power factor, these configurations are best suited for applications with low power factor such as active filtering or for driving some.

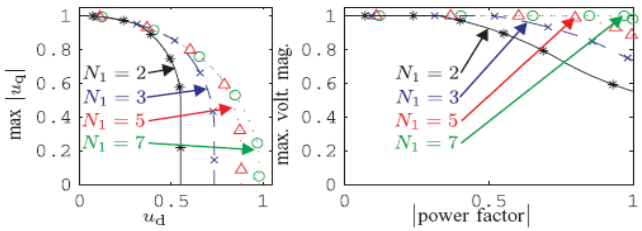


Fig. 12. Maximum theoretical approximation of the feasible operating region for various high-voltage cells: Two-level three-phase inverter (*), three-level three-phase NPC(×), five-levels three-phase inverter (_), and seven-level three phase

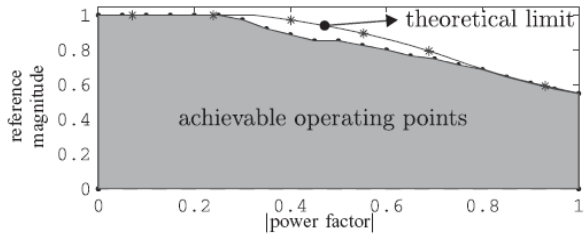


Fig.13. Gray area represents the feasible operating points that can be generated with the considered family of topologies, which combine a two-level inverter with an arbitrary number of H-bridge inverters in series such that $\Delta v1 = (M - 1)N2\Delta v2$ Induction motors. We will evaluate the performance of these configurations experimentally in the next section on an induction motor drive.

C. Fault-Handling Capability:

In this section, some aspects linked to fault-handling capabilities are briefly outlined. First, it has to be noted that a complete failure of the high-voltage cell cannot be handled as its operation is necessary to charge and balance the energy stored by the low-voltage cells. Second, if the inverter is fully hybrid, i.e., if all the cells have different voltage ratings, it will be difficult to handle a fault as all cases will require a different procedure and will need to be elaborated separately in an ad hoc way. If the inverter is designed modularly, i.e., all the cells except the large voltage cell are the same, the situation can reasonably be handled and some observations can be made. 1) Since the common mode of the low-voltage cell is already used for balancing, the margin to use it for increasing the achievable magnitude in the faulty phase, as is done in is very limited. For the same reason, it will be difficult to use the voltage of the healthy cells in a row unless the capacitor is sized to handle single-phase energy ripple. It may be simpler to switch-off all cells in the corresponding row and to operate with one row less. 2) The switches need to be oversized in voltage such as the inverter handles the load voltage after the fault and bypass modules need to be added. .

VIII. EXPERIMENTAL RESULTS

A. Experimental Setup:

1) Hardware Prototype: A modular hybrid cascaded multilevel inverter prototype has been built to validate the proposed concepts. Each module implements a three-phase cell made with three H-bridge power modules. The modules were assembled using different types of power switching devices available in the same package to test some of the topologies discussed in Section

II-A. In this paper, we present results for two three-phase PWM inverters (a) and (b) of Table II, using an association of 600-V/30 A IGBTs and 100-V/30 A MOSFETs.

These two inverter configurations are tested on a standard 230-V induction motor. It is worth noting that since the ratio between the selected switch operating voltages is 6, it would be required to adopt configuration (c) of Table II to optimally employ the selected silicon devices: the resulting topology would be suitable to supply a standard drive on a standard 400-V grid.

B.Five level hybrid Cascaded Multilevel Inverter Drive Results:

In this section, the performance of the three-phase PWM inverter configurations (a) of Table II is evaluated. This topology is as the topology in Fig. 2(b) when removing the third cell $\boldsymbol{c}3$. In this configuration, the setup is limited by the rating of the MOSFETs: applying (26d) with uDC2 =50 V and _ =5 V, the nominal high voltage cell dc voltage is obtained uDC1 ≈ 90 V.

1) Voltage Regulation during Pre charge: Fig. 14 demonstrates the good regulation of the dc voltages. Fig. 14(a) shows the pre charge of the three capacitors. During the pre charge, condition (8) is not fulfilled and it is necessary to switch the high-voltage cell at the PWM frequency.

The pre charge current and the PWM frequency are, therefore, selected smaller than their rated values (1 kHz, 2 A). *2) Voltage Regulation during Normal Operation:* Upon completion of the pre charge, in Fig. 14(b), the PWM frequency is set to 2 kHz and the high-voltage cell is switched at most at three times the fundamental frequency. In Fig. 14(b)-(d), we can see that the high-voltage cell is operated at three times the fundamental frequency at low and medium speed and at the fundamental frequency at high speed. The maximum switching

frequency is, therefore, around 60 Hz: this maximum frequency appears before the drive switches from four to two pulses per period on the line to-line voltage and when the drive operates.

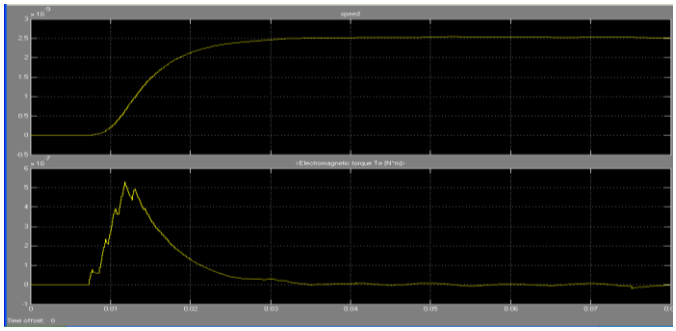


Fig.(a) Speed v/s Electromagnetic torque

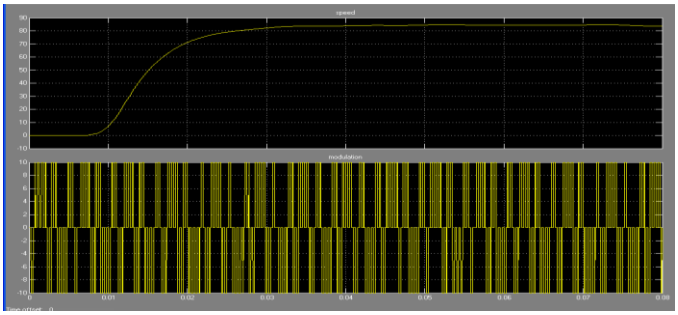


Fig.(b): Speed v/s Modulation

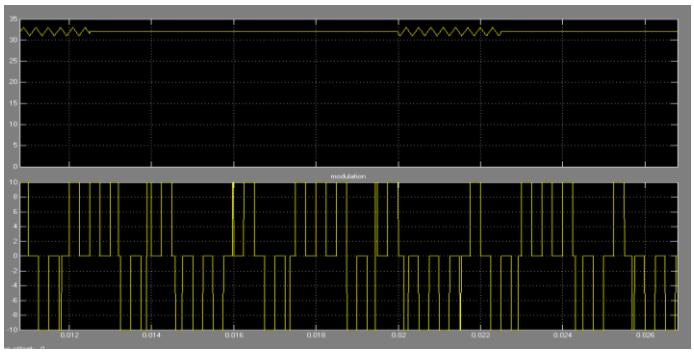


Fig.(c): Speed v/s Modulation

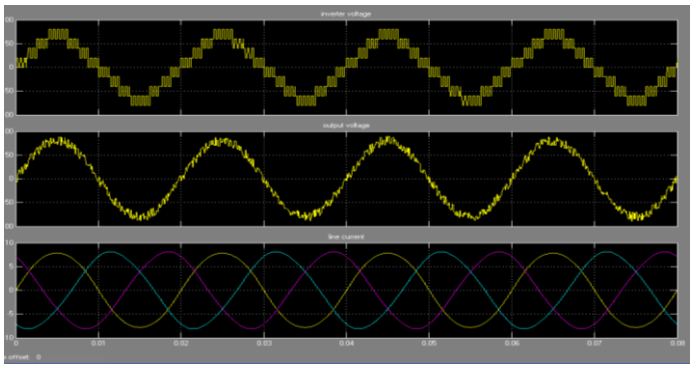


Fig.(d): Inverter voltage v/s Output voltage v/s line current

IX. CONCLUSION

Designing of hybrid cascaded multilevel inverters with simplified supply and low switching losses have been derived by using six rules. These design rules constrain the ratio between the dc voltages of the supplied cells and the dc voltages of the unsupplied cells. They allow one to design single- and three-phase inverters that can be operated either with staircase or with PWM. The concept of simplified energy domain has been introduced to characterize the achievable operating modes and power factor..The switching devices can be optimally used, which results in a very high energy efficiency and very high number of levels. The internal balance of the cells over the phases and within the phase can be decoupled from the total energy regulation. Applying the pulse width modulation and staircase concepts, the solution is suitable for high dynamic performance. The effectiveness of the proposed concepts has been demonstrated experimentally on an multilevel induction motor drive.

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